

Title	Page
Cover Sheet	1
Block Diagram	2
Device Map	3
GPIO Table	4
Clock Distribution	5
CPU:LGA 1155	6 - 10
DDR III DIMM	11 - 13
INTEL-COUGAR POINT PCH	14 - 20
IO-Fintek F71808A	21
PCIE X16 SLOT	22
PCIE X1 SLOT	23
LAN-INTEL 82579	24
Audio Codec ALC887-VD-GR	25
USB 3.0 front + rear	26 27
USB 2.0 Connector	28
USB 2.0 Power + USB3.0 Power Control	29
ACPI Controller	30
DDR Power	31
CPU (VCCP/VTT) & PCH Power	32 33
VRD12 - NCP6151S52MNR2G 4-Phase	34 35
ATX PWR-Connector/LED	36
CPU/PCH XDP	37
VGA	38
HDMI	39
Manual & Option parts	41
Power Map/History	40 42

MS-7728 Ver: 10 uATX(216mm X 244mm)

CPU:

INTEL -Sandy Bridge LGA 1155 (SOCKET H2)

System Chipset:

INTEL-H61 (COUGAR POINT)

OnBoard Chipset:

HD Audio Codec:ALC887-VD-GR

LAN:INTEL 82579 10/100/1000

IO: Fintek F71808A

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel) max:8GB

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PWM:

Controller NCP6151S52MNR2G 4-Phase -- 95W

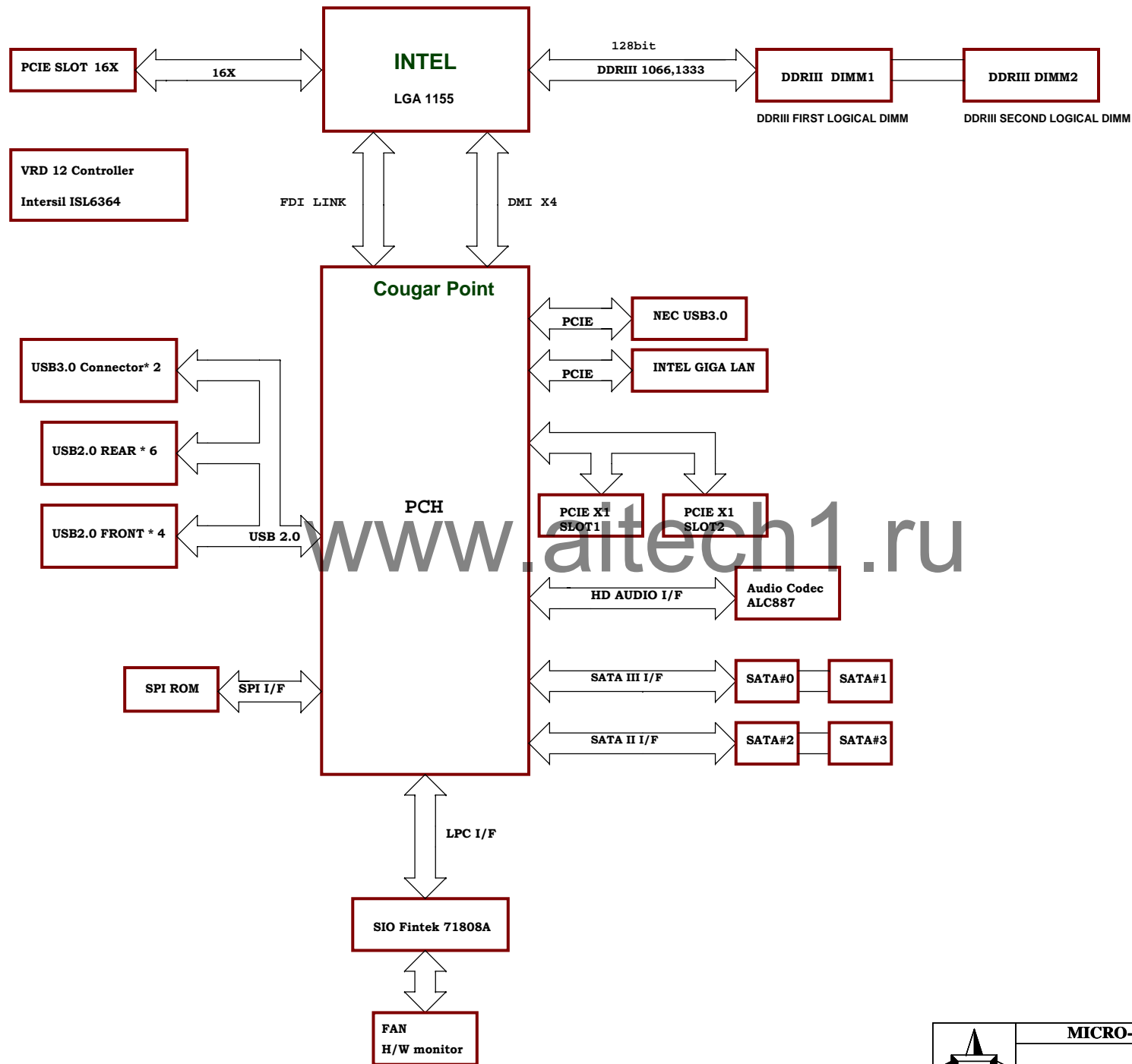
Other:

PCH-H61 SATA(SATA2-300MB/s) *4

PCH-H67 SATA(SATA2-300MB/s) *2+ (SATA3-600MB/s) *2

USB2.0 *8 (Rear*4 / Front*4)

USB3.0 *4 (Rear*2 / Front*2) rear or front select one



MICRO-STAR INT'L CO.,LTD			
MS-7728			
Size Custom	Document Description Block Diagram		Rev 10
Date: Tuesday, January 11, 2011	Sheet	2	of 42

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9↓
USB PORT-MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #2	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

				18BXPSAK GPIO DEFINITION	
GPIO	POWER	IO	Function	Implementation	Mother board Function
GPIO0	MAIN	1	BMBUSY#	10 K Pull-up to +3.3V	ADPT_ID_DET#
GPIO1	MAIN	1	TACH1	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH1
GPIO2	MAIN	1	PCLIRQB#	See PCA Spec	PCI Interrupt E#
GPIO3	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt F#
GPIO4	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt G#
GPIO5	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt H#
GPIO6	MAIN	1	TACH2	Pull-up to +3.3V and connect to P52 pin 12. The COMMM 8 assembly connects pin 12 directly to GND	COMM_8_DET#/ MOM_TH_ALRT#
GPIO7	MAIN	1	TACH3	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH3(PSU Fan Control)
GPIO8	RESUMB	0	ICG_B#		Reserved
GPIO9	RESUMB	1	OC5	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO10	RESUMB	1	OC6	10K Pull-up to +3.3V and connect to P126-pin 16	PRNTR_DET#
GPIO11	RESUMB	1	SMBALERT#	20K Pull-up to +3.3VSB. It is always enabled as a wake event.	SMBALERT#
GPIO12	RESUMB	1	LAN_DISABLE	Follow implementation in Intel Picton Design Guide	LAN_DISABLE#
GPIO13	RESUMB	1	IO_PMB	10K Pull-up to +3.3V and connect to P151-pin 10; also add a no-installed pull-down to the net.	RDYBST_DET# or DASH SMI
GPIO14	RESUMB	1	OC7	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation. 8.2K Pull-up to +3.3V and connect to the SMI pin on the SIO	SMI# from SIO
GPIO15	RESUMB	1	PCB_GPIO15		Reserved
GPIO16	RESUMB	0	SATA2DP	10 M pull-up to VBAT and connect to CPU SKT0CC#, SIO pin48 and PCH	CPU_MISSING
GPIO17	MAIN	1	TACH0	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH0(Front Chassis Fan)
GPIO18	MAIN	1	PCIECLKQ#	Through a 1KΩ series resistor, 8.2K pull-up to +3.3V and connect to E15-pin 1. E15 Pin 2 connect to GND	BOOT_BLK_REC#
GPIO19	MAIN	1	SATA1QP	connect to a test point	unused
GPIO20	MAIN	1	PCIECLKQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to HANKSVILLE -pin48	PCIECLKQ2#
GPIO21	MAIN	1	SATA2QP	10K pull-up to +3.3V and connect to P23-pin 4.	FRNT_AUD_DET#
GPIO22	MAIN	1	SCLOCK	10K Pull-up to +3.3V and connect to P160-pin 10	INT_USB_DET#
GPIO23	MAIN	1	LDQ#	connect to a test point.	PEG_MOM_DET#
GPIO24	RESUMB	0	MBALED	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to P125-Pin 1. 1M pull-up to VBAT and connect to P125-pin 3	HOOD_SW_DET#
GPIO25	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKQ3#
GPIO26	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKQ4#
GPIO27	RESUMB	0	OD_PLL_VR_EN	10K pull-up to +3.3VAUX	Reserved
GPIO28	RESUMB	0	PCB_GP28	connect to a test point	unused
GPIO29	RESUMB	0	SLP_LAN#	refer to the PCA spec.	SLP_LAN#
GPIO30	RESUMB	1	SUS_PWRACK	100K Pull-up to 3V_AUX	unused
GPIO31	MAIN	1	ACPRESENT	10K Pull-up to +3.3V and connect to P25-pin 10	FRONT_USB_DET1#
GPIO32	MAIN	0	PCB_GP32	Through a 1kΩ series resistor, 10K pull-up to +3.3V and connect to P2-pin 6.	NON-EPA_PS_DET#

GPIO33	MAIN	0	PCB_GP33	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to pin 1 of jumper E1 and E1 pin2 to GND	FDT_OVRD#
GPIO34	MAIN	0	SP_PC#	3.3K Pull-down to GND and connect to P124-pin 2. Decouple P124-pin 2 with 0.1μF P124 pin 1 2.2K pull-up to 5V and P124 pin 6 2.2k pull-up to 5V	HOOD_LOCK_DET
GPIO35	MAIN	0	SATACLKREQ#	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0
GPIO36	MAIN	1	SATA2QP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1
GPIO37	MAIN	1	SATA3QP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2
GPIO38	MAIN	1	SLOAD	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 9. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID0
GPIO39	MAIN	1	SDATAOUT0	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	BRD_ID1
GPIO40	RESUMB	1	OC1	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for XDP implementation. 8.2kΩ pull-down to GND and connect to E49-pin 2 E49 pin-1 300 pull-up to +3.3V	PASSWORD_EN
GPIO41	RESUMB	1	OC2	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO42	RESUMB	1	OC3	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO43	RESUMB	1	OC4	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO44	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3VAUX and connect to a test point.	PCIECLKQ6#
GPIO45	RESUMB	1	PCIECLKQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J3-pin8 I7	PRSN#_J31
GPIO46	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKQ7#
GPIO47	RESUMB	1	PBG_A_CLKQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J4-pin848 and B81	PRSN#_J41
GPIO48	MAIN	1	SDATAOUT1	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 10. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID1
GPIO49	MAIN	0	SATA3QP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0
GPIO50	MAIN	1	PCLRBQ#1	8.2k pull-up to VCC3	REQ1#
GPIO51	MAIN	0	PCLQNT#1	connect to a test point	GNT1#
GPIO52	MAIN	1	PCLRBQ#2	8.2k pull-up to VCC3	REQ2#
GPIO53	MAIN	0	PCLQNT#2	connect to a test point	GNT2#
GPIO54	MAIN	1	PCLRBQ#3	Through a 8.2KΩ series resistor, connect to E14-pin 2 and 1K pull-down to GND. E14-pin1 connect to +3.3V	BOOT_BLK_EN#
GPIO55	MAIN	0	PCLQNT#3	connect to a test point	GNT3#
GPIO56	RESUMB	1	PBG_B_CLKQ#	refer to the PCA spec.	AUD_AMP_DIS#
GPIO57	MAIN	1	PCB_GP57	10K Pull-up to +3.3VME installed and 10K pull-down to GND not installed.	TPM_PP

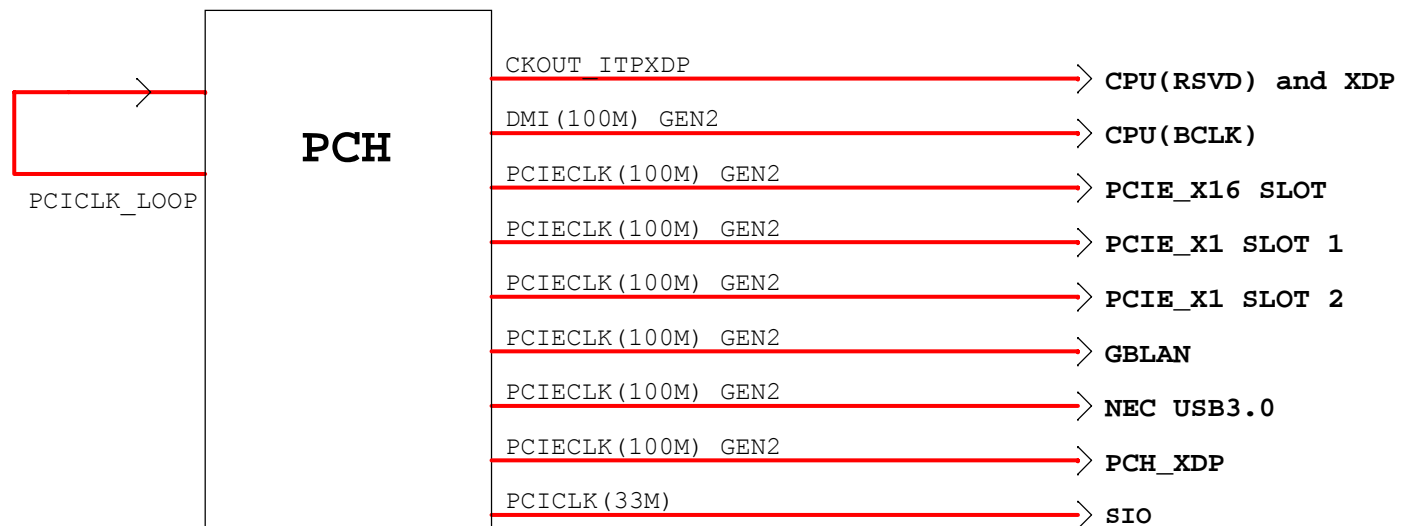
GPIO58	RESUMB	0	SMCLK	10K pull-up to 3V_AUX	SMCLK
GPIO59	RESUMB	1	OC0	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO60	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALARM
GPIO61	RESUMB	0	SUS_STAT#	connect to a test pin	LPCPD#
GPIO62	RESUMB	0	SUSCLK	SUSCLK to SIO-pin16	SUSCLK
GPIO63	RESUMB	0	SLP_S#	Connect to the SIO-pin37	SLP_S#
GPIO64	MAIN	0	CLKOUTFLBK0	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK0
GPIO65	MAIN	0	CLKOUTFLBK1	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK1
GPIO66	MAIN	0	CLKOUTFLBK2	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK2
GPIO67	MAIN	0	CLKOUTFLBK3	refer to the PCA spec. unused clock connect to a test point	CLK14M
GPIO72	RESUMB	1	PCB_GP72	Pull-up to +3.3V and connect to P24-pin 10	FRONT_USB_DET0#
GPIO73	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3VAUX and through a 0Ω series resistor, connect to J42-pin8 I7, B31, B48, and B81	PRSN#_J42
GPIO74	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALERT#
GPIO75	RESUMB	0	SMDLIDATA	10K pull-up to 3V_AUX	SMDLIDATA



MICRO-STAR INT'L CO.,LTD

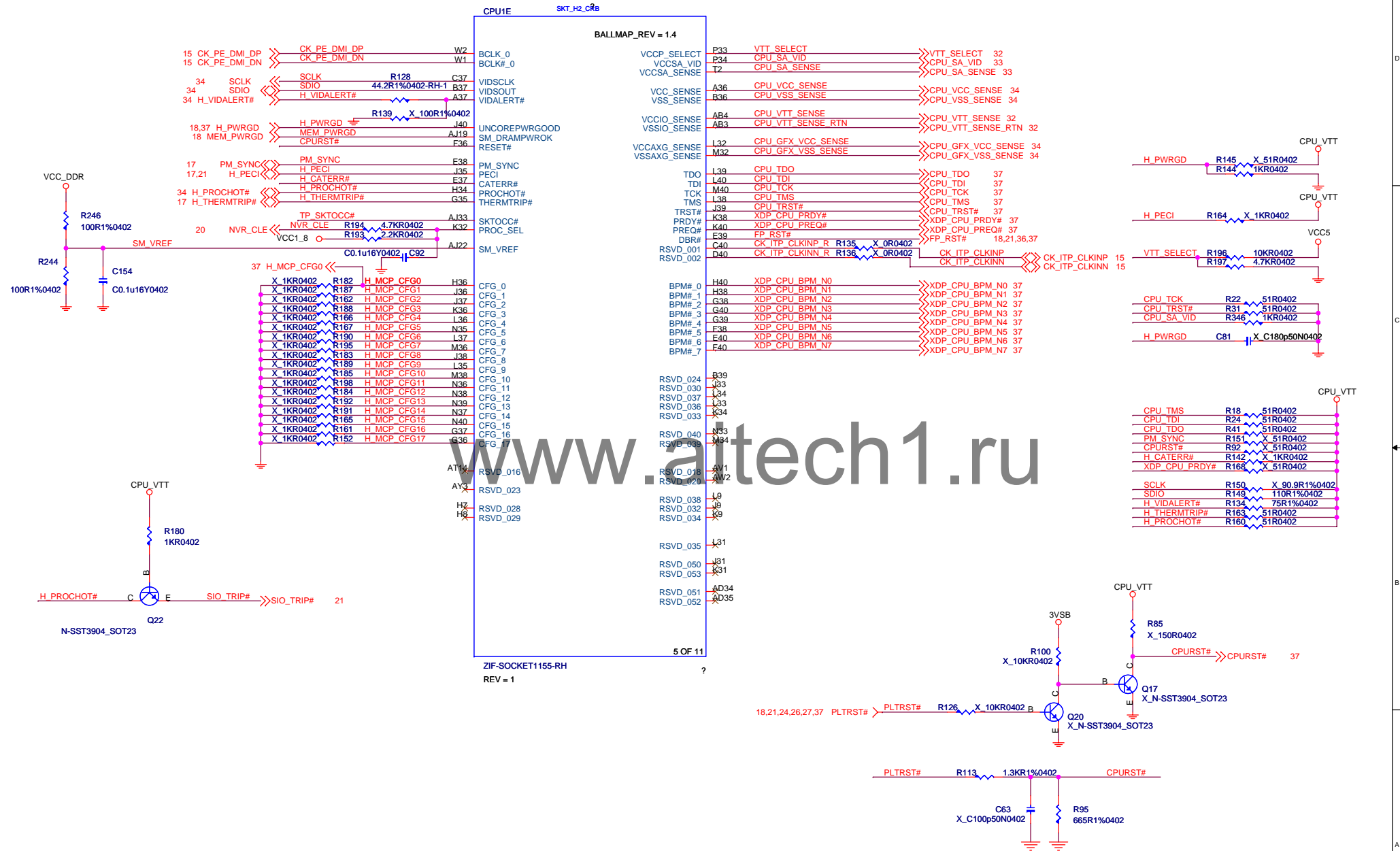
MS-7728

Size Custom	Document Description	Rev
	PCH GPIO Table	10
Date: Tuesday, January 11, 2011		Sheet 4 of 42

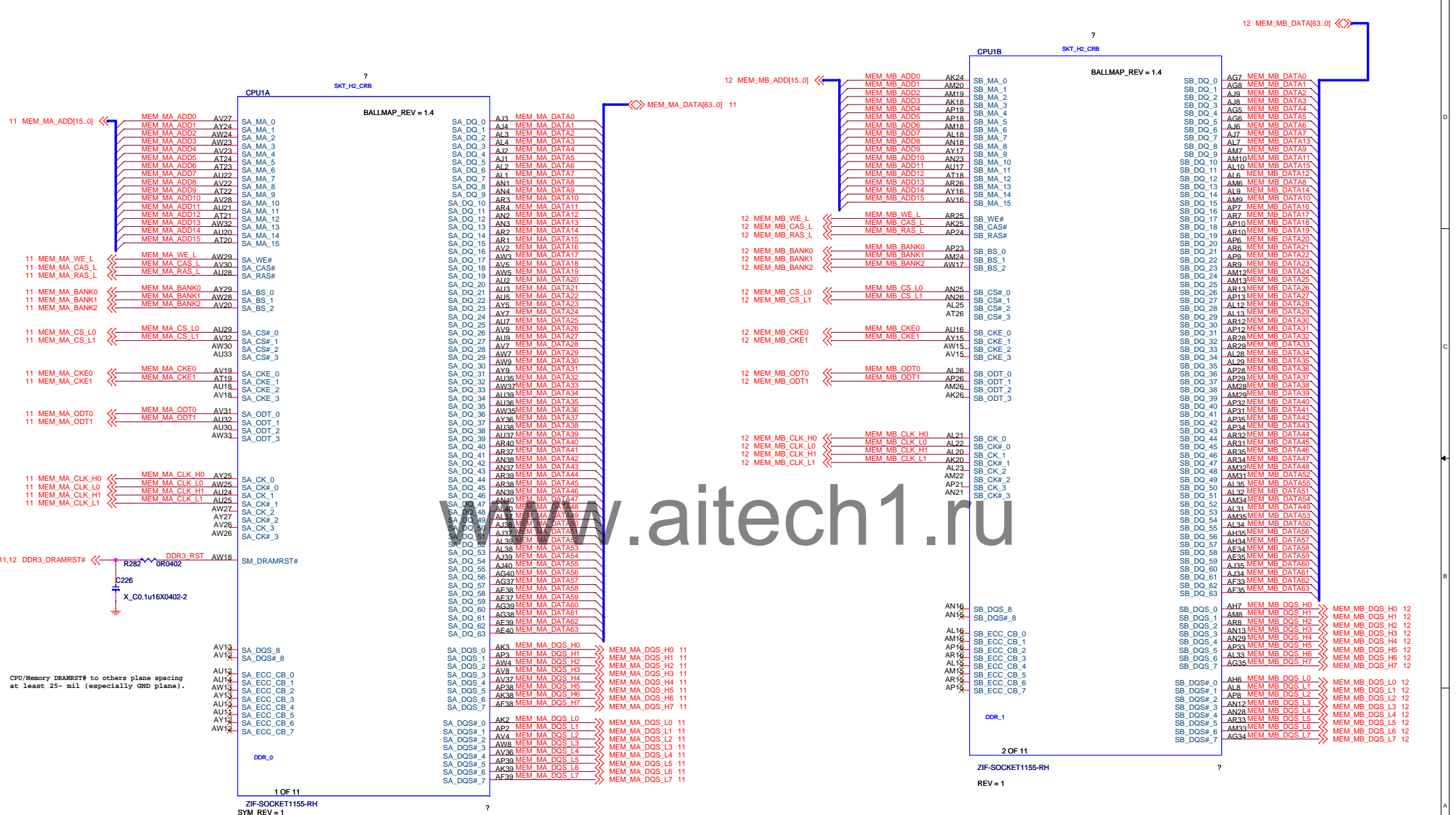


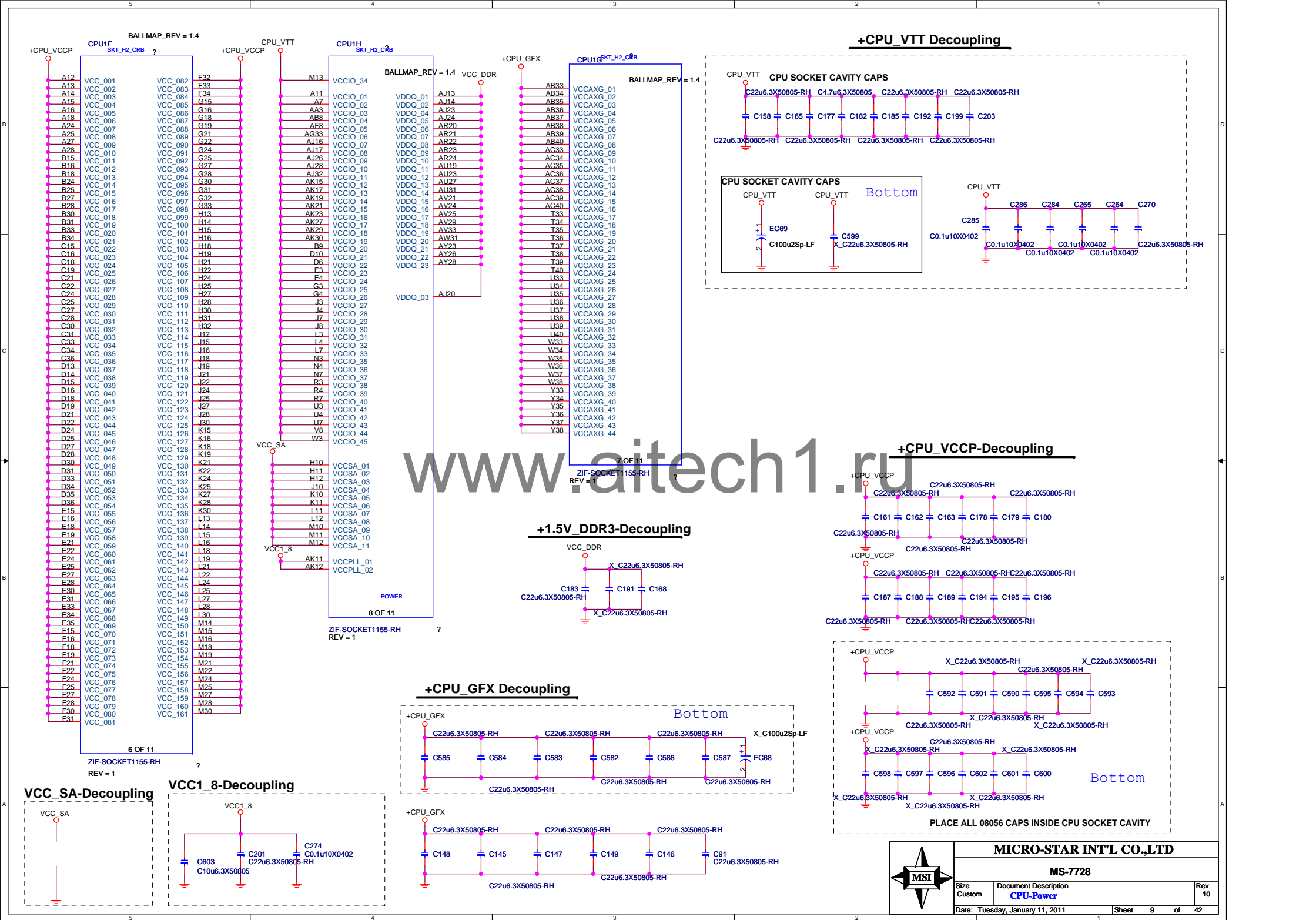
X'TAL
25 MHz

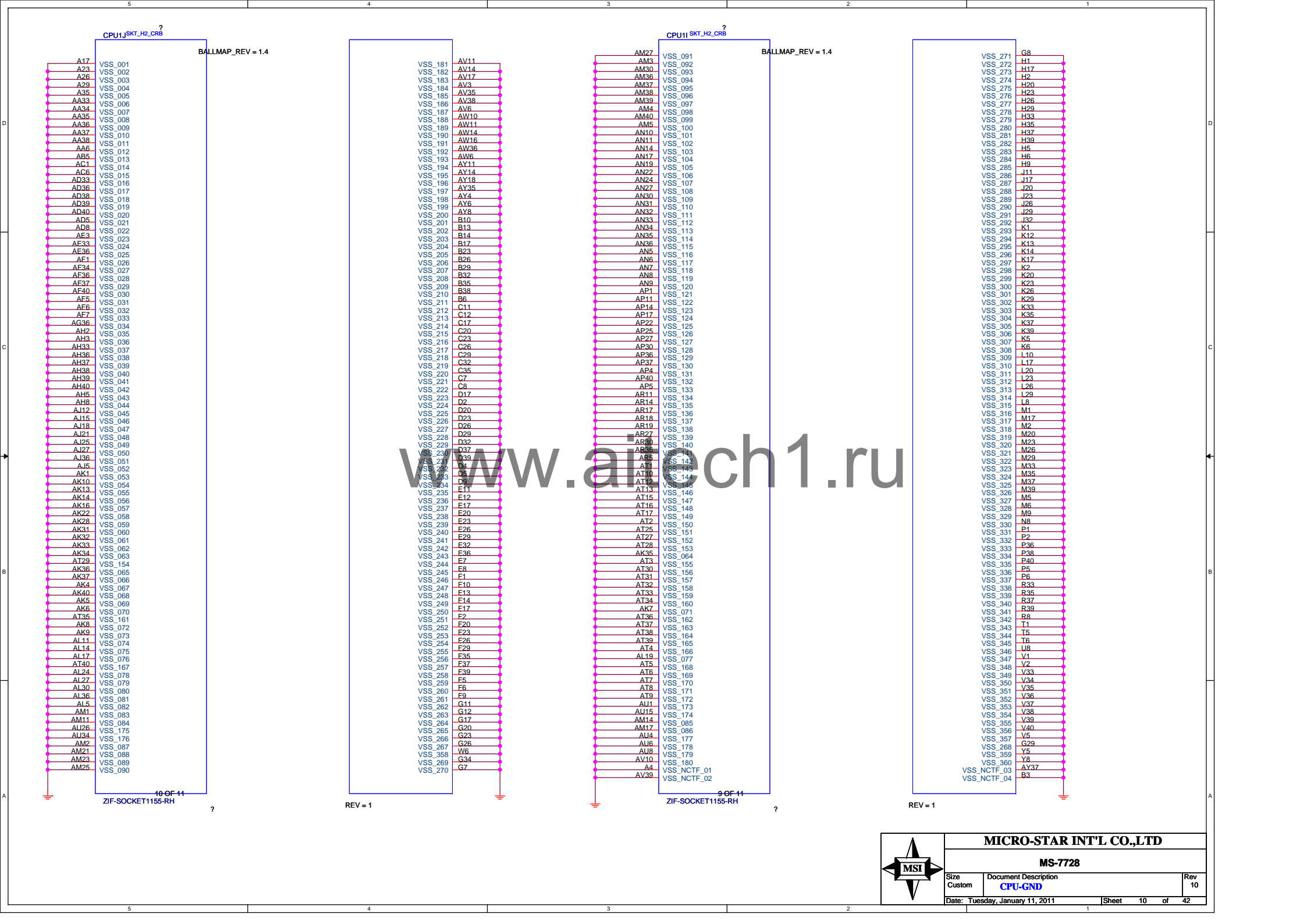
www.aitech1.ru



MICRO-STAR INT'L CO.,LTD			
MS-7728			
Size	Document Description		Rev
Custom	CPU-CLK/Control/MISC		10
Date: Tuesday, January 11, 2011		Sheet 6 of 42	

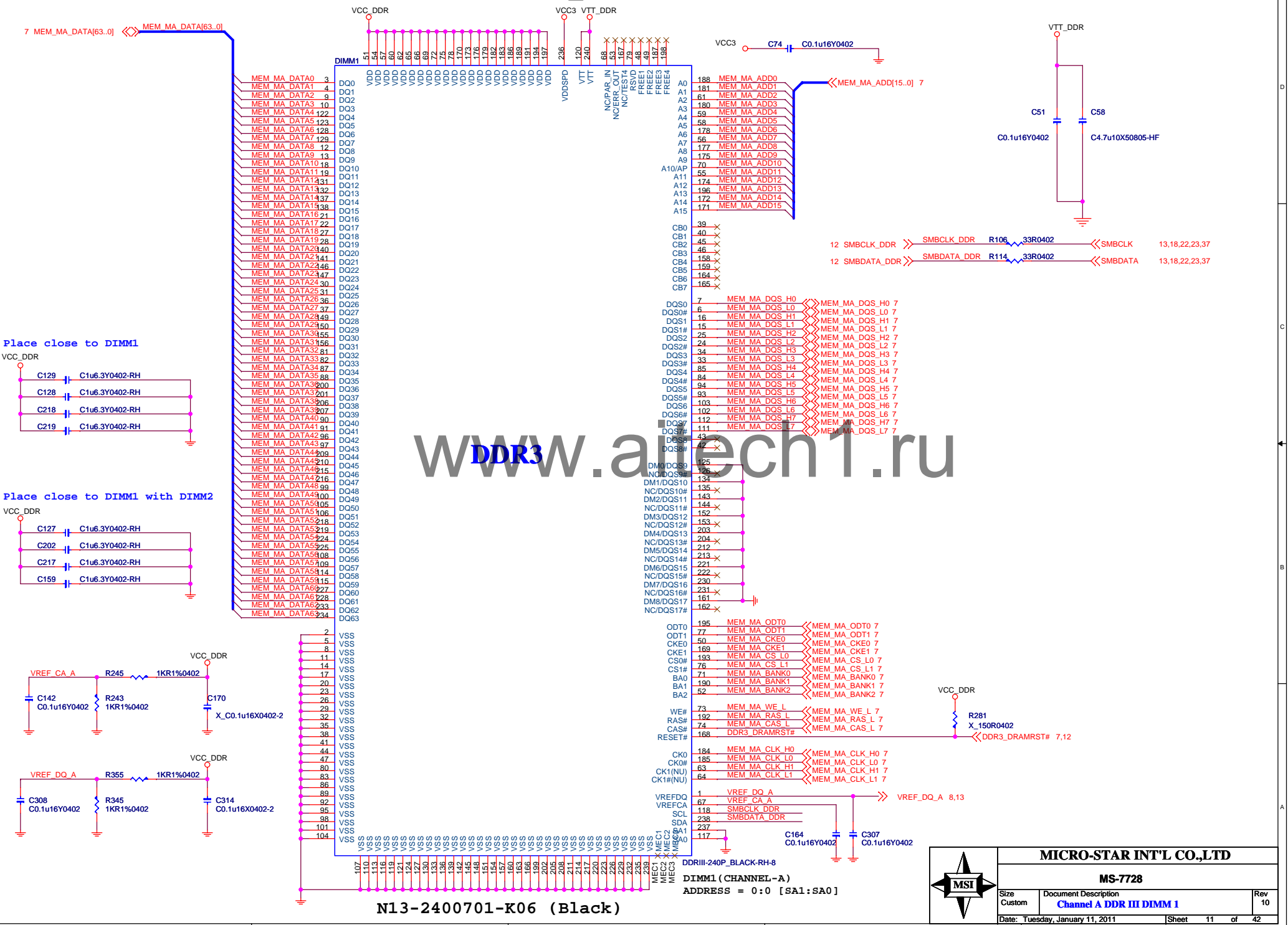




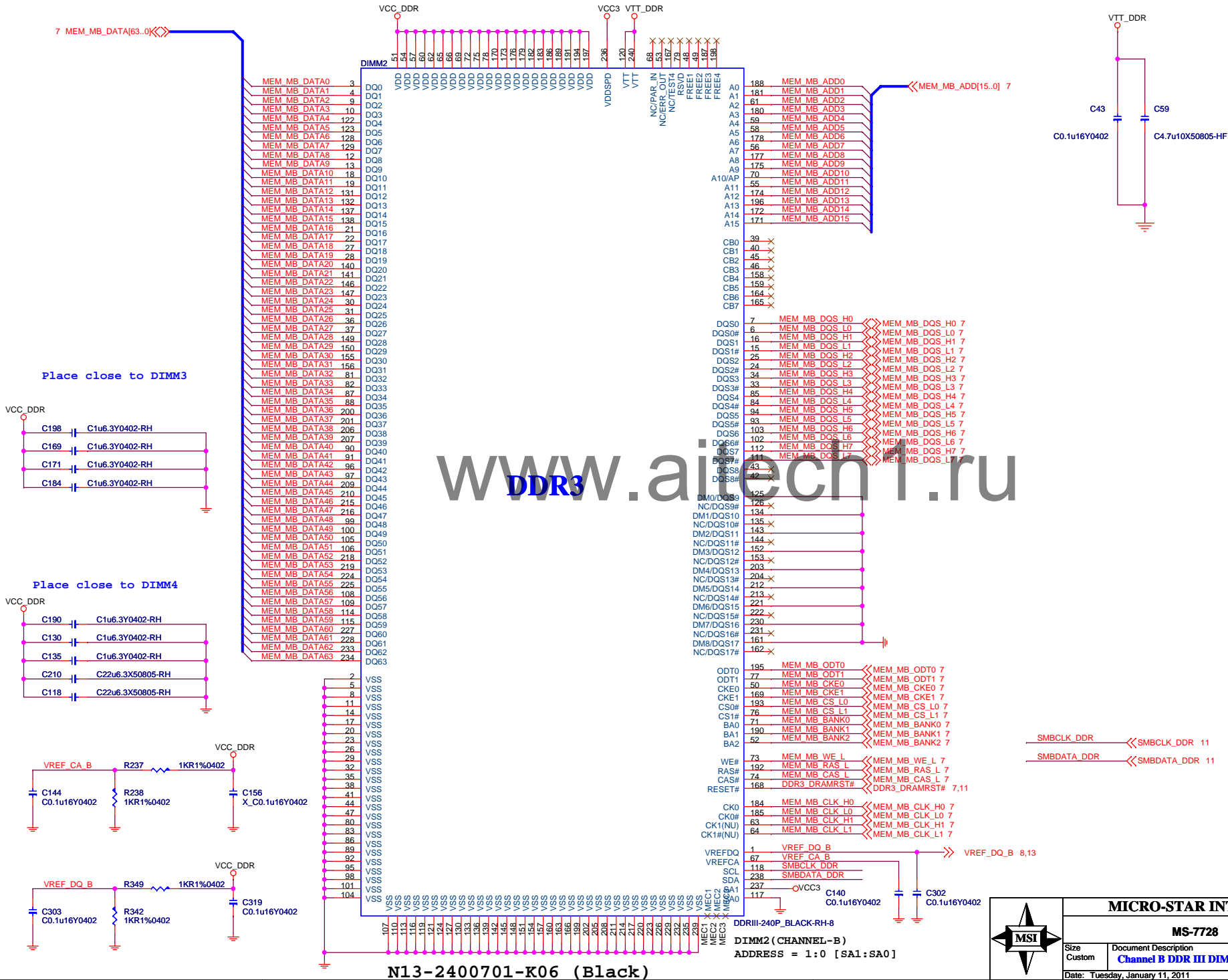


MICRO-STAR INT'L CO.,LTD		
MS-7728		
Size Custom	Document Description CPU-GND	Rev 10
Date: Tuesday, January 11, 2011		Sheet 10 of 42

DDRIII DIMM_A1



DDRIII DIMM_B1



N13-2400701-K06 (Black)

DDRIII-240P_BLACK-RH-8

DIMM2 (CHANNEL-B)

ADDRESS = 1:0 [SA1:SA0]

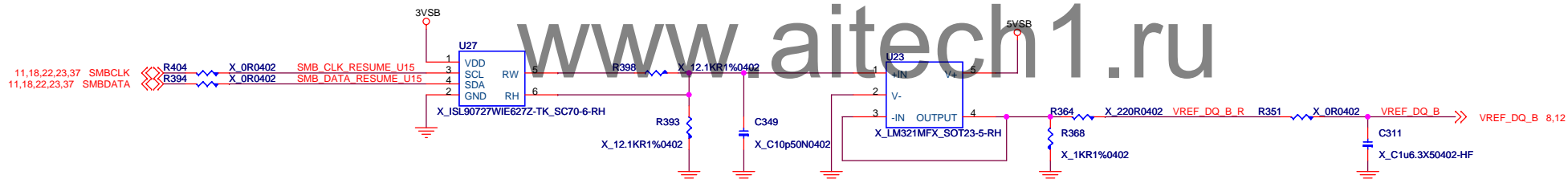
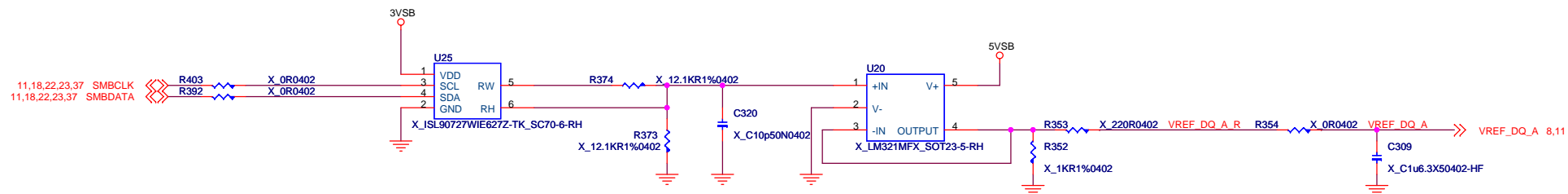


MICRO-STAR INT'L CO.,LTD

MS-7728

Size	Document Description	Rev
Custom	Channel B DDR III DIMM 3	10
Date:	Tuesday, January 11, 2011	Sheet 12 of 42

www.aitech1.ru



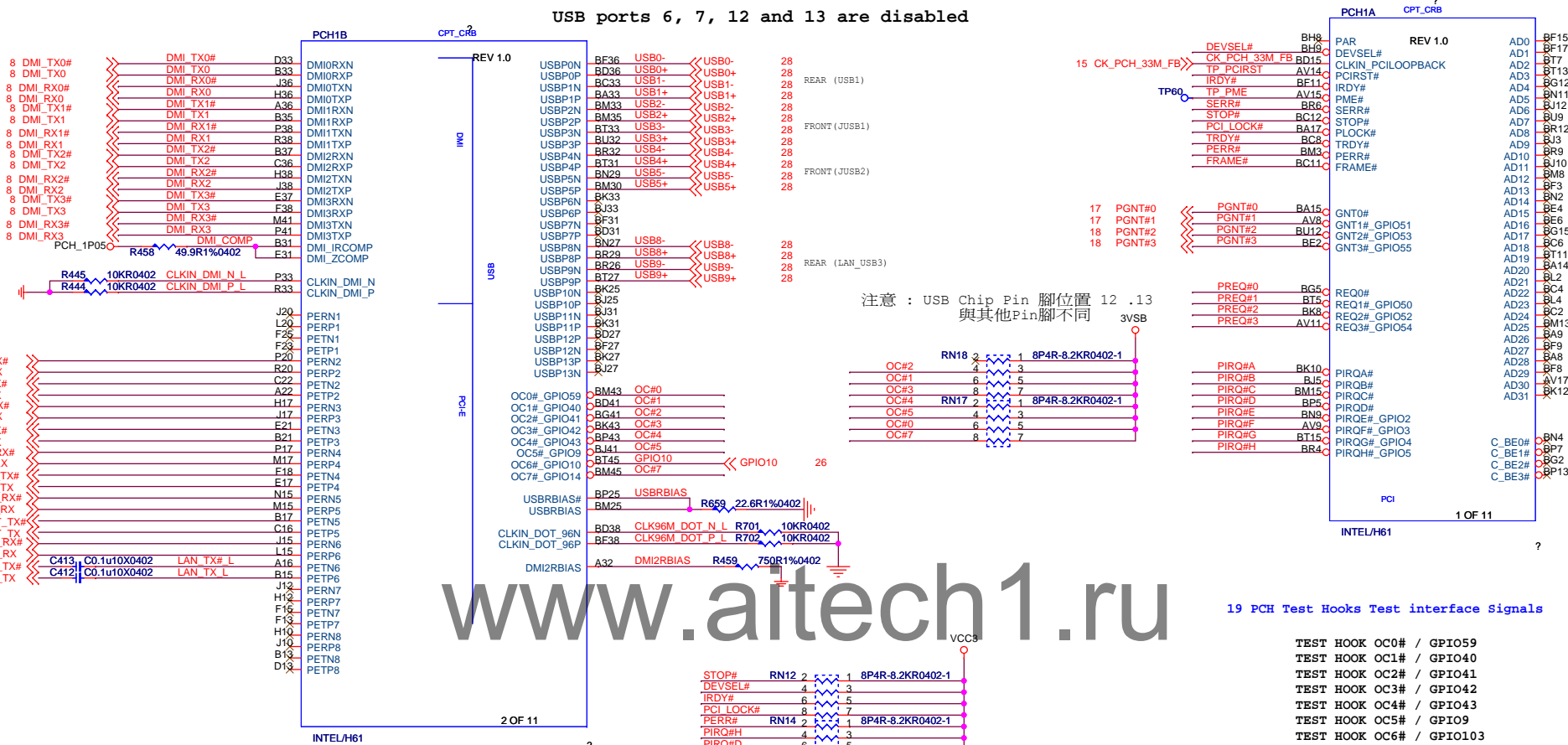
MICRO-STAR INT'L CO.,LTD

MS-7728

Size Custom	Document Description DIMM VREF (Option)	Rev 10
Date: Tuesday, January 11, 2011		
Sheet 13 of 42		

H61

USB ports 6, 7, 12 and 13 are disabled



H61

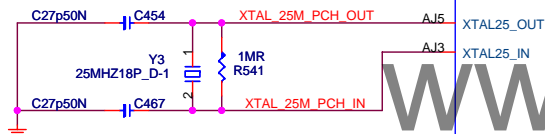
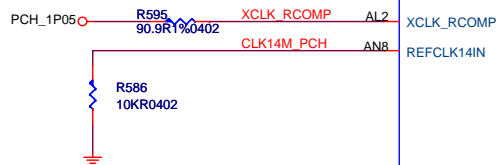
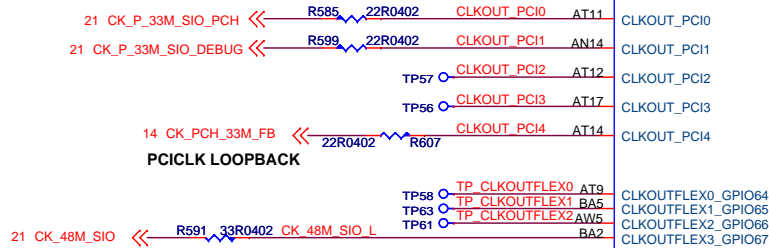
PCIe ports 7 and 8 are disabled.



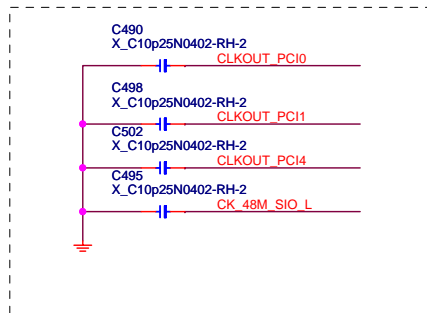
MICRO-STAR INT'L CO.,LTD

MS-7728

Size	Document Description	Rev
Custom	PCI-E/DMI/USB	10
Date: Tuesday, January 11, 2011	Sheet 14 of 42	

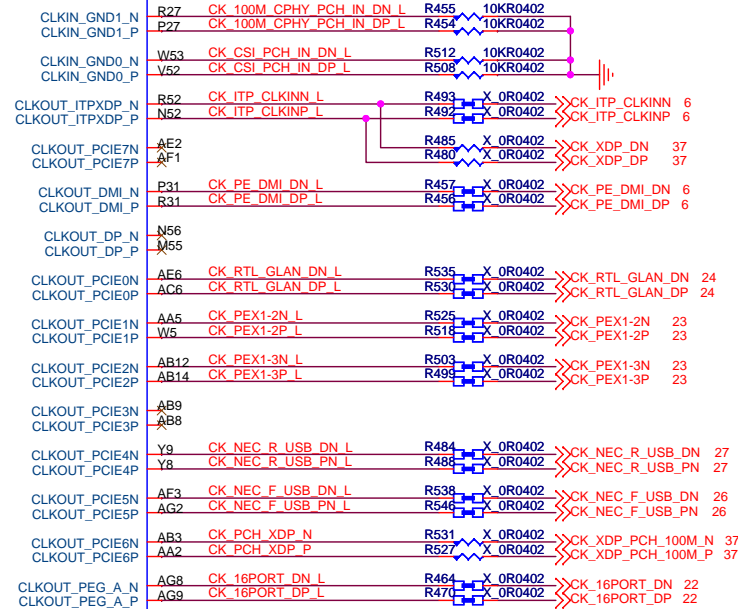


EMI Result



PCH1H CPT_CRB ?

REV 1.0



8 OF 11

INTEL/H61



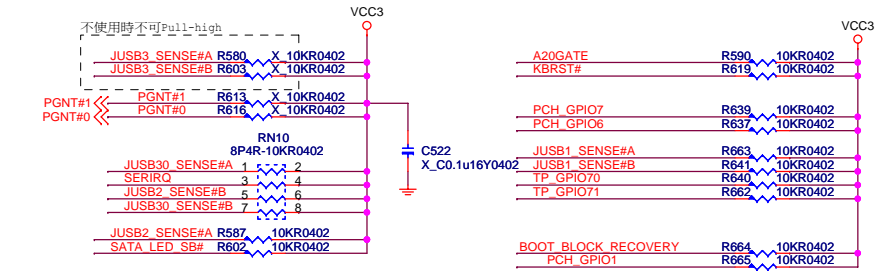
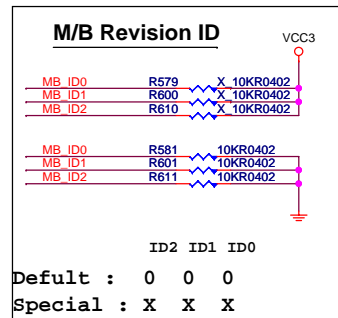
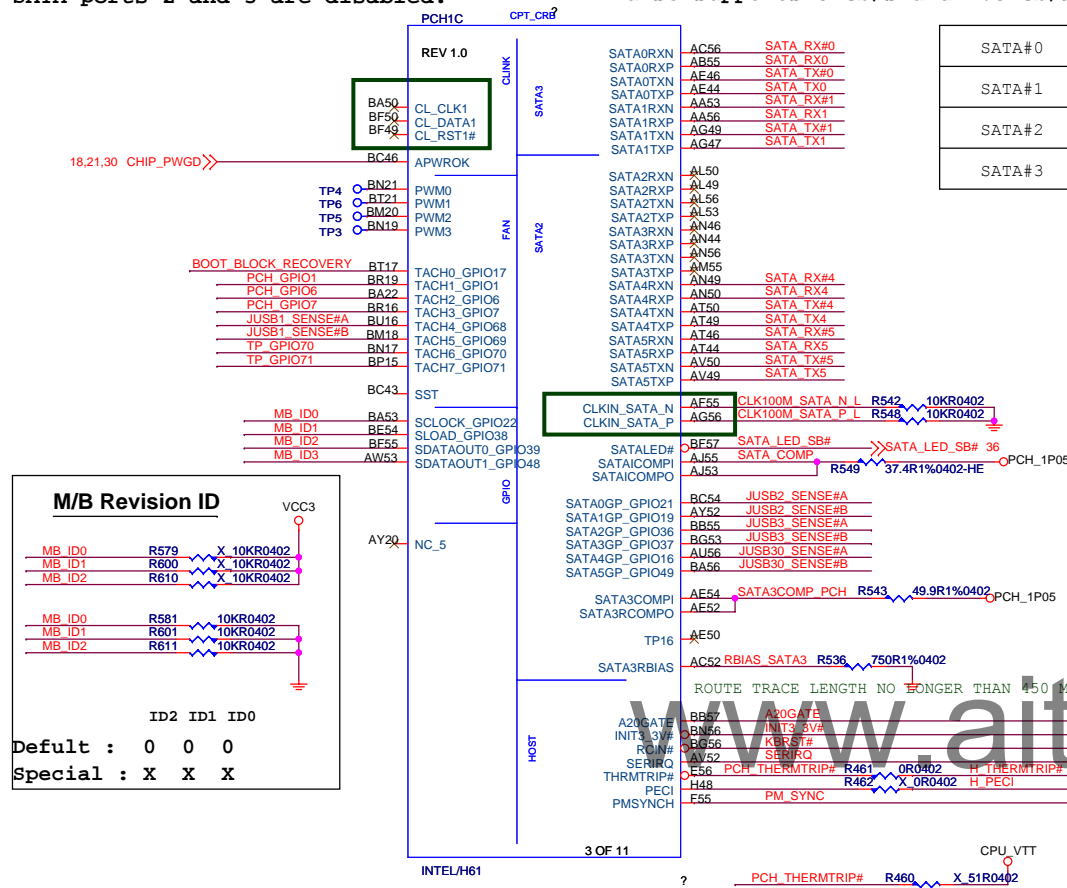
MICRO-STAR INT'L CO.,LTD

MS-7728

Size	Document Description	Rev
B	PCH-CLOCK	10
Date:	Tuesday, January 11, 2011	Sheet 15 of 42

H61
SATA ports 2 and 3 are disabled.

SATA 6 Gb/s support on port 0 only. SATA port 0
also supports 3 Gb/s and 1.5 Gb/s.

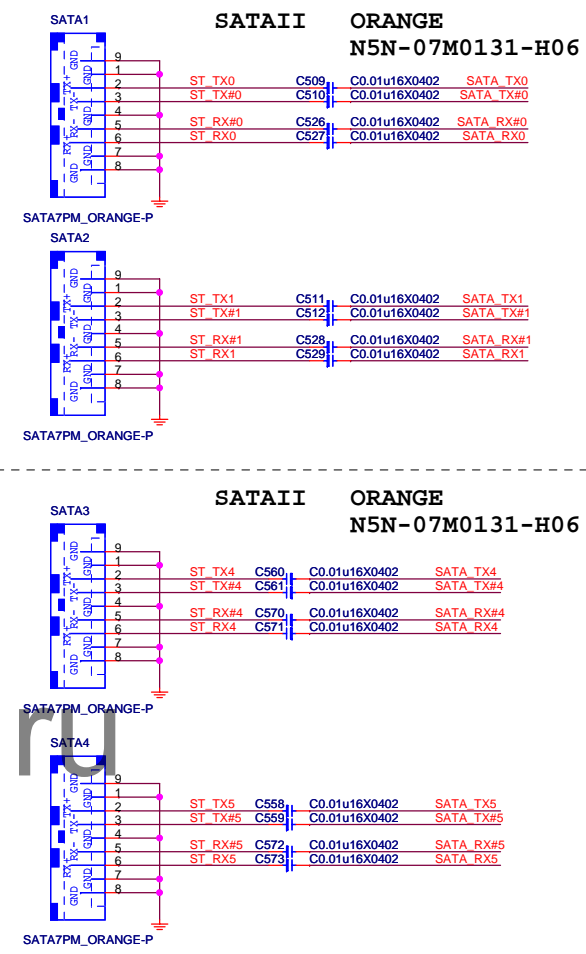


BOOT DEVICE	GNT1#/GPIO51	SATA1GP/GPIO19
SPI	floating	floating
PCI	0	floating
LPC	0	0

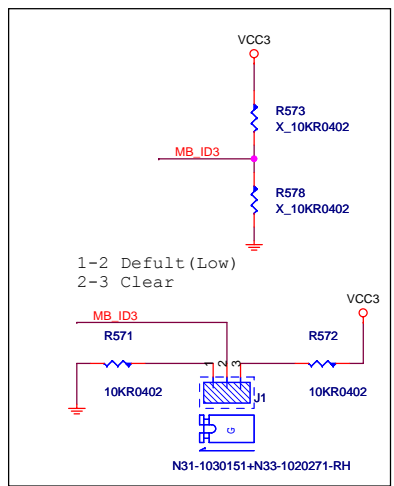
Balls have an internal weak pull-up - Default destination is SPI

SATA#0	Primary Master
SATA#1	Secondary Master
SATA#2	Primary Slave
SATA#3	Secondary Slave

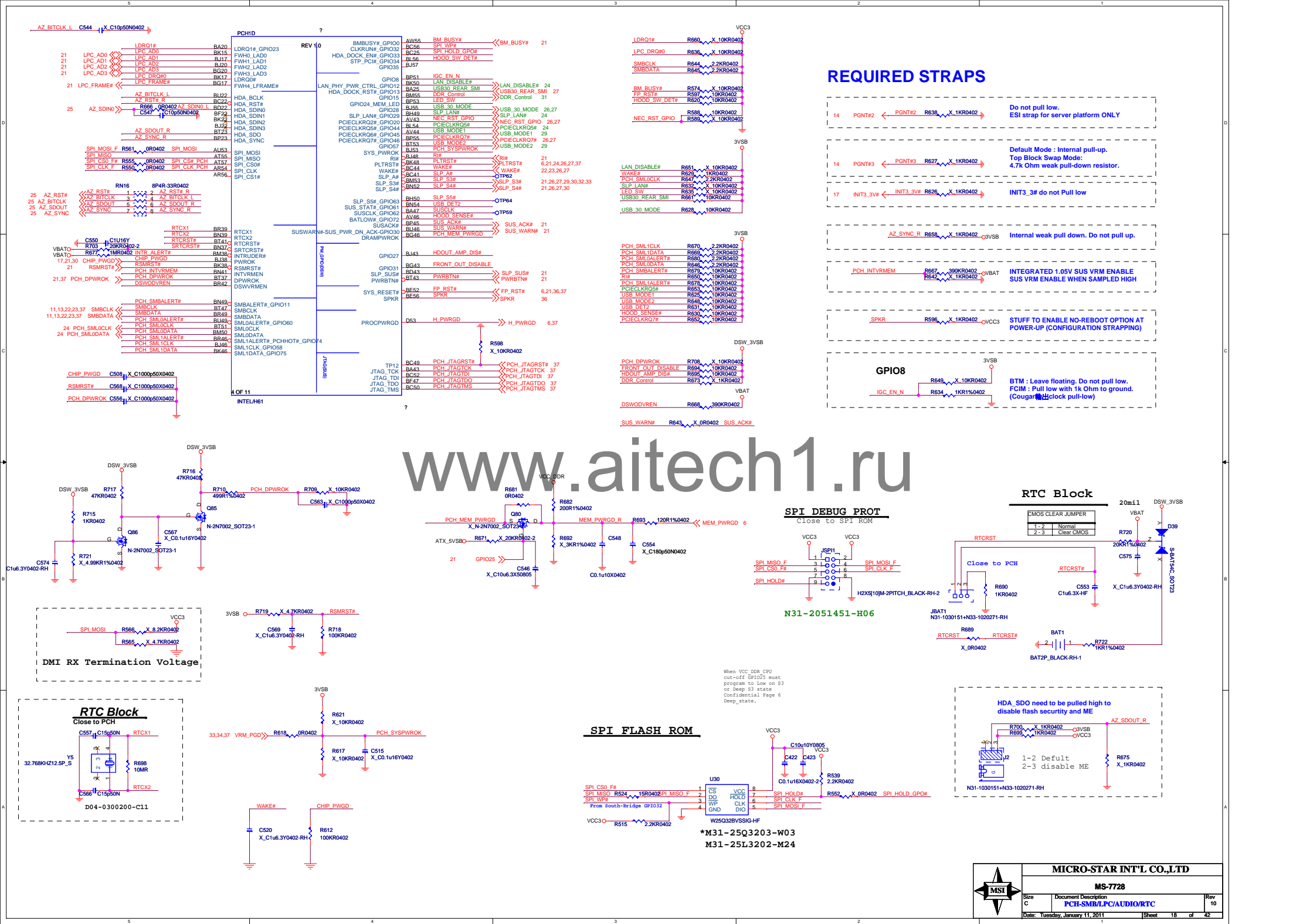
SATA connector



Clear PASS-Word Jumper



MICRO-STAR INT'L CO.,LTD		
MS-7728		
Size Custom	Document Description PCH-SATA/HOST/FAN/GPIO	Rev 10
Date: Tuesday, January 11, 2011	Sheet 17	of 42



OPT_008

BC15	VSS_0125
BC16	VSS_0126
BC17	VSS_0127
BC18	VSS_0128
BC19	VSS_0129
BC20	VSS_0130
BC21	VSS_0131
BC22	VSS_0132
BC23	VSS_0133
BC24	VSS_0134
BC25	VSS_0135
BC26	VSS_0136
BC27	VSS_0137
BC28	VSS_0138
BC29	VSS_0139
BC30	VSS_0140
BC31	VSS_0141
BC32	VSS_0142
BC33	VSS_0143
BC34	VSS_0144
BC35	VSS_0145
BC36	VSS_0146
BC37	VSS_0147
BC38	VSS_0148
BC39	VSS_0149
BC40	VSS_0150
BC41	VSS_0151
BC42	VSS_0152
BC43	VSS_0153
BC44	VSS_0154
BC45	VSS_0155
BC46	VSS_0156
BC47	VSS_0157
BC48	VSS_0158
BC49	VSS_0159
BC50	VSS_0160
BC51	VSS_0161
BC52	VSS_0162
BC53	VSS_0163
BC54	VSS_0164
BC55	VSS_0165
BC56	VSS_0166
BC57	VSS_0167
BC58	VSS_0168
BC59	VSS_0169
BC60	VSS_0170
BC61	VSS_0171
BC62	VSS_0172
BC63	VSS_0173
BC64	VSS_0174
BC65	VSS_0175
BC66	VSS_0176
BC67	VSS_0177
BC68	VSS_0178
BC69	VSS_0179
BC70	VSS_0180
BC71	VSS_0181
BC72	VSS_0182
BC73	VSS_0183
BC74	VSS_0184
BC75	VSS_0185
BC76	VSS_0186
BC77	VSS_0187
BC78	VSS_0188
BC79	VSS_0189
BC80	VSS_0190
BC81	VSS_0191
BC82	VSS_0192
BC83	VSS_0193
BC84	VSS_0194
BC85	VSS_0195
BC86	VSS_0196
BC87	VSS_0197
BC88	VSS_0198
BC89	VSS_0199
BC90	VSS_0200
BC91	VSS_0201
BC92	VSS_0202
BC93	VSS_0203
BC94	VSS_0204
BC95	VSS_0205
BC96	VSS_0206
BC97	VSS_0207
BC98	VSS_0208
BC99	VSS_0209
BC00	VSS_0210
BC01	VSS_0211
BC02	VSS_0212
BC03	VSS_0213
BC04	VSS_0214
BC05	VSS_0215
BC06	VSS_0216
BC07	VSS_0217
BC08	VSS_0218
BC09	VSS_0219
BC10	VSS_0220
BC11	VSS_0221
BC12	VSS_0222
BC13	VSS_0223
BC14	VSS_0224
BC15	VSS_0225
BC16	VSS_0226
BC17	VSS_0227
BC18	VSS_0228
BC19	VSS_0229
BC20	VSS_0230

VSS_0004	AV22
VSS_0005	AE56
VSS_0006	BR36
VSS_0007	AV17
VSS_0008	BR36
VSS_0009	NC_1
VSS_0010	NC_2
VSS_0011	NC_3
VSS_0012	NC_4
VSS_0013	NC_5
VSS_0014	NC_6
VSS_0015	NC_7
VSS_0016	NC_8
VSS_0017	NC_9
VSS_0018	NC_10
VSS_0019	NC_11
VSS_0020	NC_12
VSS_0021	NC_13
VSS_0022	NC_14
VSS_0023	NC_15
VSS_0024	NC_16
VSS_0025	NC_17
VSS_0026	NC_18
VSS_0027	NC_19
VSS_0028	NC_20
VSS_0029	NC_21
VSS_0030	NC_22
VSS_0031	NC_23
VSS_0032	NC_24
VSS_0033	NC_25
VSS_0034	NC_26
VSS_0035	NC_27
VSS_0036	NC_28
VSS_0037	NC_29
VSS_0038	NC_30
VSS_0039	NC_31
VSS_0040	NC_32
VSS_0041	NC_33
VSS_0042	NC_34
VSS_0043	NC_35
VSS_0044	NC_36
VSS_0045	NC_37
VSS_0046	NC_38
VSS_0047	NC_39
VSS_0048	NC_40
VSS_0049	NC_41
VSS_0050	NC_42
VSS_0051	NC_43
VSS_0052	NC_44
VSS_0053	NC_45
VSS_0054	NC_46
VSS_0055	NC_47
VSS_0056	NC_48
VSS_0057	NC_49
VSS_0058	NC_50
VSS_0059	NC_51
VSS_0060	NC_52
VSS_0061	NC_53
VSS_0062	NC_54
VSS_0063	NC_55
VSS_0064	NC_56
VSS_0065	NC_57
VSS_0066	NC_58
VSS_0067	NC_59
VSS_0068	NC_60
VSS_0069	NC_61
VSS_0070	NC_62
VSS_0071	NC_63
VSS_0072	NC_64
VSS_0073	NC_65
VSS_0074	NC_66
VSS_0075	NC_67
VSS_0076	NC_68
VSS_0077	NC_69
VSS_0078	NC_70
VSS_0079	NC_71
VSS_0080	NC_72
VSS_0081	NC_73
VSS_0082	NC_74
VSS_0083	NC_75
VSS_0084	NC_76
VSS_0085	NC_77
VSS_0086	NC_78
VSS_0087	NC_79
VSS_0088	NC_80
VSS_0089	NC_81
VSS_0090	NC_82
VSS_0091	NC_83
VSS_0092	NC_84
VSS_0093	NC_85
VSS_0094	NC_86
VSS_0095	NC_87
VSS_0096	NC_88
VSS_0097	NC_89
VSS_0098	NC_90
VSS_0099	NC_91
VSS_0100	NC_92
VSS_0101	NC_93
VSS_0102	NC_94
VSS_0103	NC_95
VSS_0104	NC_96
VSS_0105	NC_97
VSS_0106	NC_98
VSS_0107	NC_99
VSS_0108	NC_100
VSS_0109	NC_101
VSS_0110	NC_102
VSS_0111	NC_103
VSS_0112	NC_104
VSS_0113	NC_105
VSS_0114	NC_106
VSS_0115	NC_107
VSS_0116	NC_108
VSS_0117	NC_109
VSS_0118	NC_110
VSS_0119	NC_111
VSS_0120	NC_112
VSS_0121	NC_113
VSS_0122	NC_114
VSS_0123	NC_115
VSS_0124	NC_116
VSS_0125	NC_117
VSS_0126	NC_118
VSS_0127	NC_119
VSS_0128	NC_120
VSS_0129	NC_121
VSS_0130	NC_122
VSS_0131	NC_123
VSS_0132	NC_124
VSS_0133	NC_125
VSS_0134	NC_126
VSS_0135	NC_127
VSS_0136	NC_128
VSS_0137	NC_129
VSS_0138	NC_130
VSS_0139	NC_131
VSS_0140	NC_132
VSS_0141	NC_133
VSS_0142	NC_134
VSS_0143	NC_135
VSS_0144	NC_136
VSS_0145	NC_137
VSS_0146	NC_138
VSS_0147	NC_139
VSS_0148	NC_140
VSS_0149	NC_141
VSS_0150	NC_142
VSS_0151	NC_143
VSS_0152	NC_144
VSS_0153	NC_145
VSS_0154	NC_146
VSS_0155	NC_147
VSS_0156	NC_148
VSS_0157	NC_149
VSS_0158	NC_150
VSS_0159	NC_151
VSS_0160	NC_152
VSS_0161	NC_153
VSS_0162	NC_154
VSS_0163	NC_155
VSS_0164	NC_156
VSS_0165	NC_157
VSS_0166	NC_158
VSS_0167	NC_159
VSS_0168	NC_160
VSS_0169	NC_161
VSS_0170	NC_162
VSS_0171	NC_163
VSS_0172	NC_164
VSS_0173	NC_165
VSS_0174	NC_166
VSS_0175	NC_167
VSS_0176	NC_168
VSS_0177	NC_169
VSS_0178	NC_170
VSS_0179	NC_171
VSS_0180	NC_172
VSS_0181	NC_173
VSS_0182	NC_174
VSS_0183	NC_175
VSS_0184	NC_176
VSS_0185	NC_177
VSS_0186	NC_178
VSS_0187	NC_179
VSS_0188	NC_180
VSS_0189	NC_181
VSS_0190	NC_182
VSS_0191	NC_183
VSS_0192	NC_184
VSS_0193	NC_185
VSS_0194	NC_186
VSS_0195	NC_187
VSS_0196	NC_188
VSS_0197	NC_189
VSS_0198	NC_190
VSS_0199	NC_191
VSS_0200	NC_192
VSS_0201	NC_193
VSS_0202	NC_194
VSS_0203	NC_195
VSS_0204	NC_196
VSS_0205	NC_197
VSS_0206	NC_198
VSS_0207	NC_199
VSS_0208	NC_200
VSS_0209	NC_201
VSS_0210	NC_202
VSS_0211	NC_203
VSS_0212	NC_204
VSS_0213	NC_205
VSS_0214	NC_206
VSS_0215	NC_207
VSS_0216	NC_208
VSS_0217	NC_209
VSS_0218	NC_210
VSS_0219	NC_211
VSS_0220	NC_212
VSS_0221	NC_213
VSS_0222	NC_214
VSS_0223	NC_215
VSS_0224	NC_216
VSS_0225	NC_217
VSS_0226	NC_218
VSS_0227	NC_219
VSS_0228	NC_220
VSS_0229	NC_221
VSS_0230	NC_222

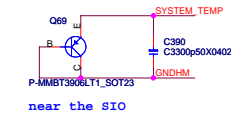
PCH1J
INTEL#61
REV 1.0
?
?
10 OF 11

OPT_008

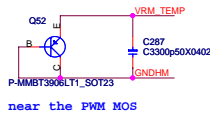
VSS_0005	AG26
VSS_0006	AG27
VSS_0007	AG28
VSS_0008	AG29
VSS_0009	AG30
VSS_0010	AG31
VSS_0011	AG32
VSS_0012	AG33
VSS_0013	AG34
VSS_0014	AG35
VSS_0015	AG36
VSS_0016	AG37
VSS_0017	AG38
VSS_0018	AG39
VSS_0019	AG40
VSS_0020	AG41
VSS_0021	AG42
VSS_0022	AG43
VSS_0023	AG44
VSS_0024	AG45
VSS_0025	AG46
VSS_0026	AG47
VSS_0027	AG48
VSS_0028	AG49
VSS_0029	AG50
VSS_0030	AG51
VSS_0031	AG52
VSS_0032	AG53
VSS_0033	AG54
VSS_0034	AG55
VSS_0035	AG56
VSS_0036	AG57
VSS_0037	AG58
VSS_0038	AG59
VSS_0039	AG60
VSS_0040	AG61
VSS_0041	AG62
VSS_0042	AG63
VSS_0043	AG64
VSS_0044	AG65
VSS_0045	AG66
VSS_0046	AG67
VSS_0047	AG68
VSS_0048	AG69
VSS_0049	AG70
VSS_0050	AG71
VSS_0051	AG72
VSS_0052	AG73
VSS_0053	AG74
VSS_0054	AG75
VSS_0055	AG76
VSS_0056	AG77
VSS_0057	AG78
VSS_0058	AG79
VSS_0059	AG80
VSS_0060	AG81
VSS_0061	AG82
VSS_0062	AG83
VSS_0063	AG84
VSS_0064	AG85
VSS_0065	AG86
VSS_0066	AG87
VSS_0067	AG88
VSS_0068	AG89
VSS_0069	AG90
VSS_0070	AG91
VSS_0071	AG92
VSS_0072	AG93
VSS_0073	AG94
VSS_0074	AG95
VSS_0075	AG96
VSS_0076	AG97
VSS_0077	AG98
VSS_0078	AG99
VSS_0079	AG100
VSS_0080	AG101
VSS_0081	AG102
VSS_0082	AG103
VSS_0083	AG104
VSS_0084	AG105
VSS_0085	AG106
VSS_0086	AG107
VSS_0087	AG108
VSS_0088	AG109
VSS_0089	AG110
VSS_0090	AG111
VSS_0091	AG112
VSS_0092	AG113
VSS_0093	AG114
VSS_0094	AG115
VSS_0095	AG116
VSS_0096	AG117
VSS_0097	AG118
VSS_0098	AG119
VSS_0099	AG120
VSS_0100	AG121
VSS_0101	AG122
VSS_0102	AG123
VSS_0103	AG124
VSS_0104	AG125
VSS_0105	AG126
VSS_0106	AG127
VSS_0107	AG128
VSS_0108	AG129
VSS_0109	AG130
VSS_0110	AG131
VSS_0111	AG132
VSS_0112	AG133
VSS_0113	AG134
VSS_0114	AG135
VSS_0115	AG136
VSS_0116	AG137
VSS_0117	AG138
VSS_0118	AG139
VSS_0119	AG140
VSS_0120	AG141
VSS_0121	AG142
VSS_0122	AG143
VSS_0123	AG144
VSS_0124	AG145
VSS_0125	AG146
VSS_0126	AG147
VSS_0127	AG148
VSS_0128	AG149
VSS_0129	AG150
VSS_0130	AG151
VSS_0131	AG152
VSS_0132	AG153
VSS_0133	AG154
VSS_0134	AG155
VSS_0135	AG156
VSS_0136	AG157
VSS_0137	AG158
VSS_0138	AG159
VSS_0139	AG160
VSS_0140	AG161
VSS_0141	AG162
VSS_0142	AG163
VSS_0143	AG164
VSS_0144	AG165
VSS_0145	AG166
VSS_0146	AG167
VSS_0147	AG168
VSS_0148	AG169
VSS_0149	AG170
VSS_0150	AG171
VSS_0151	AG172
VSS_0152	AG173
VSS_0153	AG174
VSS_0154	AG175
VSS_0155	AG176
VSS_0156	AG177
VSS_0157	AG178
VSS_0158	AG179
VSS_0159	AG180
VSS_0160	AG181
VSS_0161	AG182
VSS_0162	AG183
VSS_0163	AG184
VSS_0164	AG185
VSS_0165	AG186
VSS_0166	AG187
VSS_0167	AG188
VSS_0168	AG189
VSS_0169	AG190
VSS_0170	AG191
VSS_0171	AG192
VSS_0172	AG193
VSS_0173	AG194
VSS_0174	AG195
VSS_0175	AG196
VSS_0176	AG197
VSS_0177	AG198
VSS_0178	AG199
VSS_0179	AG200
VSS_0180	AG201
VSS_0181	AG202
VSS_0182	AG203
VSS_0183	AG204
VSS_0184	AG205
VSS_0185	AG206
VSS_0186	AG207
VSS_0187	AG208
VSS_0188	AG209
VSS_0189	AG210
VSS_0190	AG211
VSS_0191	AG212
VSS_0192	AG213
VSS_0193	AG214
VSS_0194	AG215
VSS_0195	AG216
VSS_0196	AG217
VSS_0197	AG218
VSS_0198	AG219
VSS_0199	AG220
VSS_0200	AG221

SIO Fintek 71808A

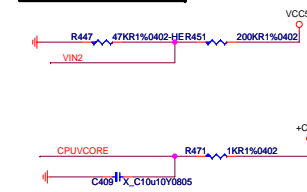
SIO TEMP



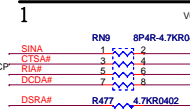
VRM TEMP



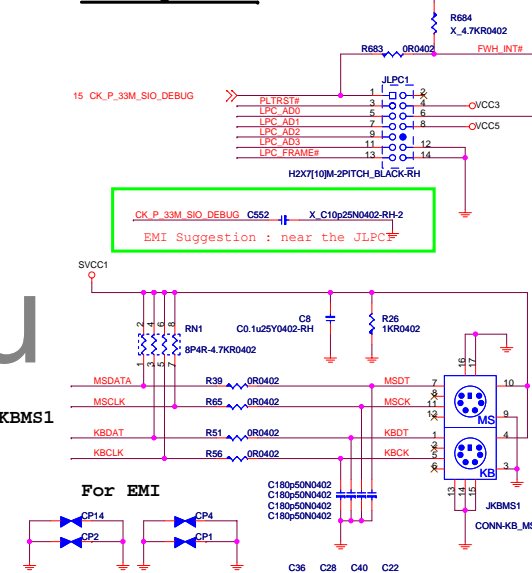
Voltage Detect



SERIAL PORT

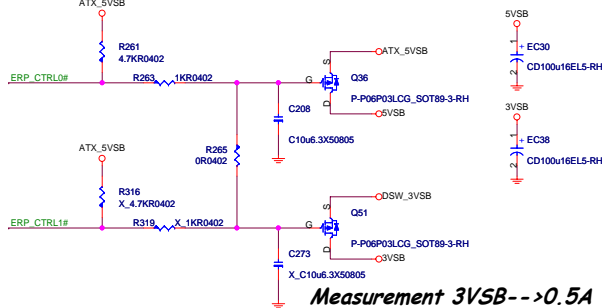


LPC Debug Port

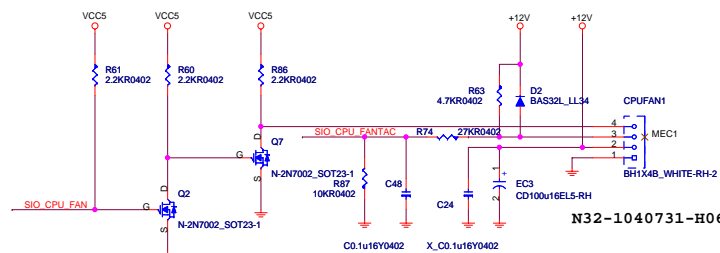


DSW POWER CONTROL

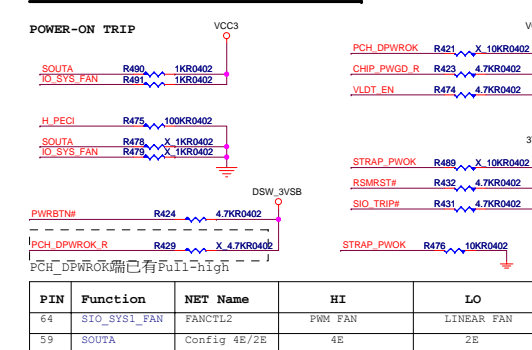
Measurement ATX_5VSB
S5:0.2A S3:0.3A



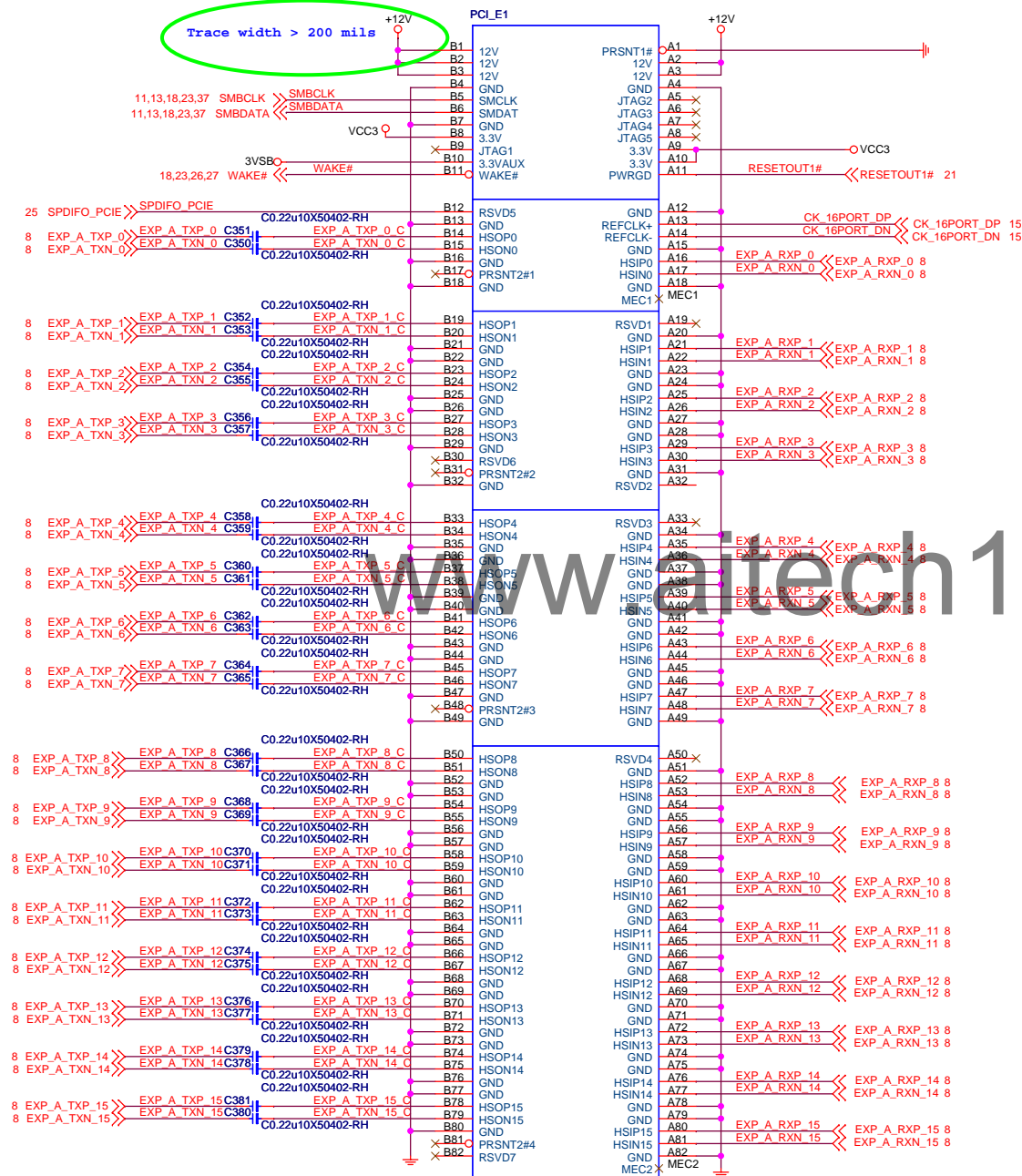
FAN-COUNTING CIRCUIT



LPC I/O STRAPPING RESISTOR



PCI Express X16 Slot



SLOT-PCI164P_BLACK-2PITCH-RH-16

N11-1640551-K06

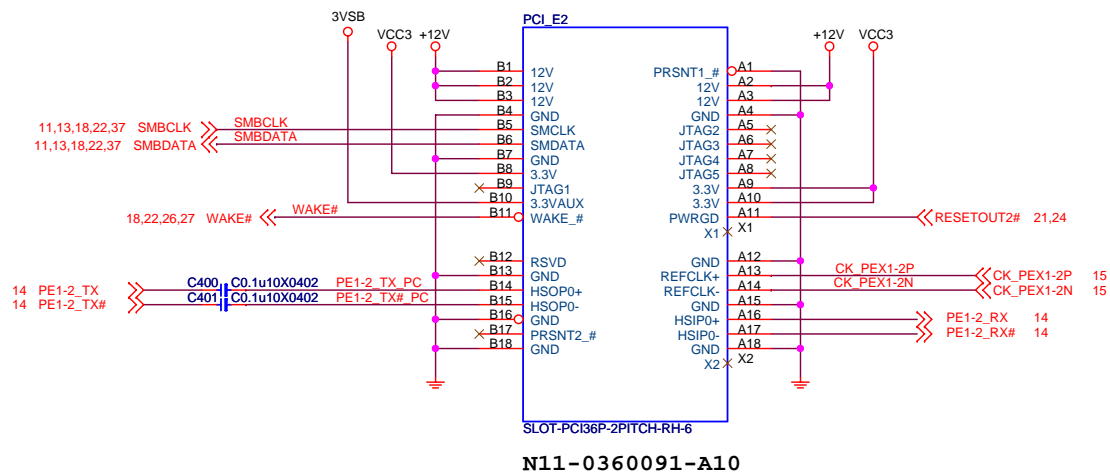


MICRO-STAR INT'L CO.,LTD

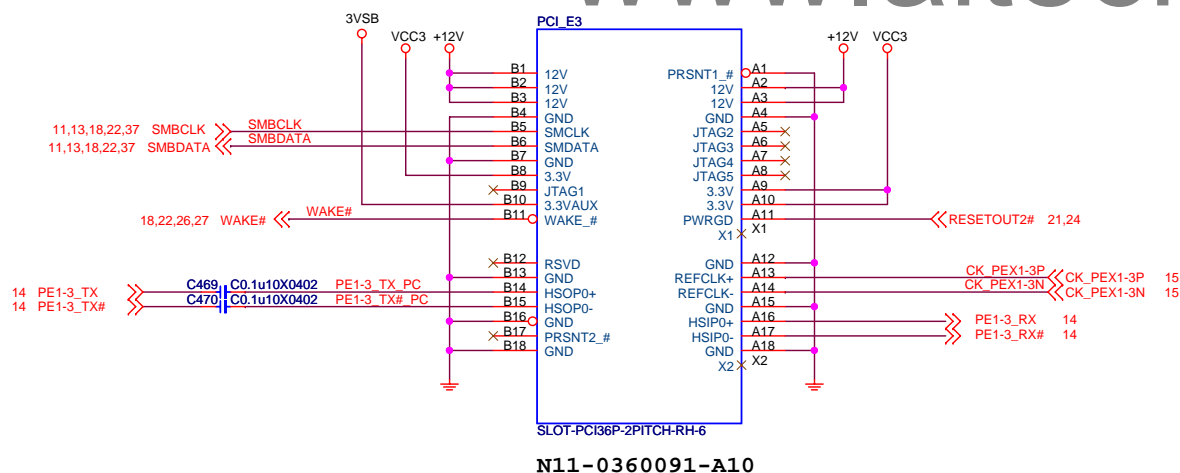
MS-7728

Size	Document Description	Rev
Custom	PCIE X16 SLOT	10
Date: Tuesday, January 11, 2011	Sheet 22 of 42	

PCI EXPRESS x1-PORT1



PCI EXPRESS x1-PORT2



MICRO-STAR INT'L CO.,LTD

MS-7728

Size
B

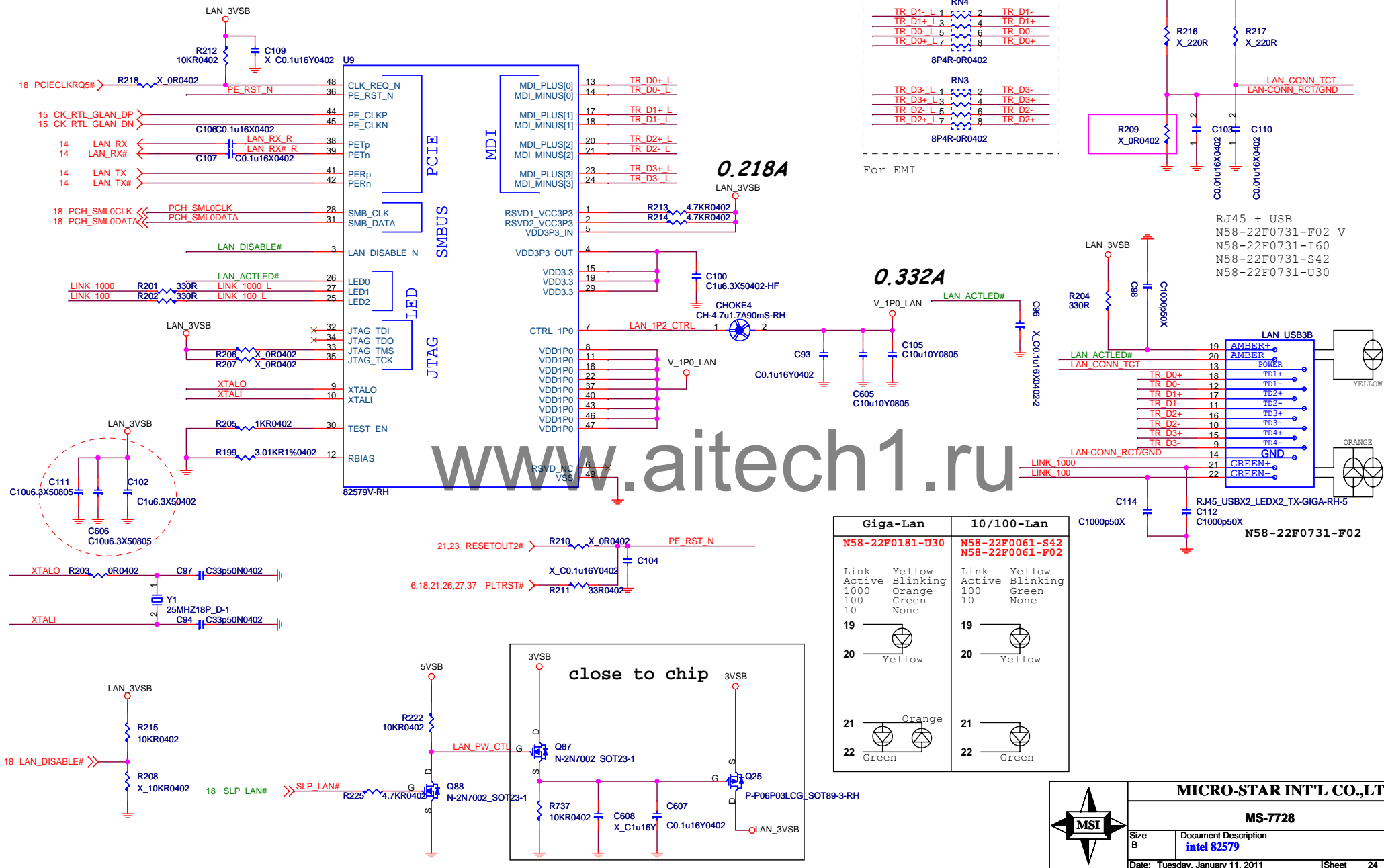
Document Description
PCIe X1 SLOT

Rev
10

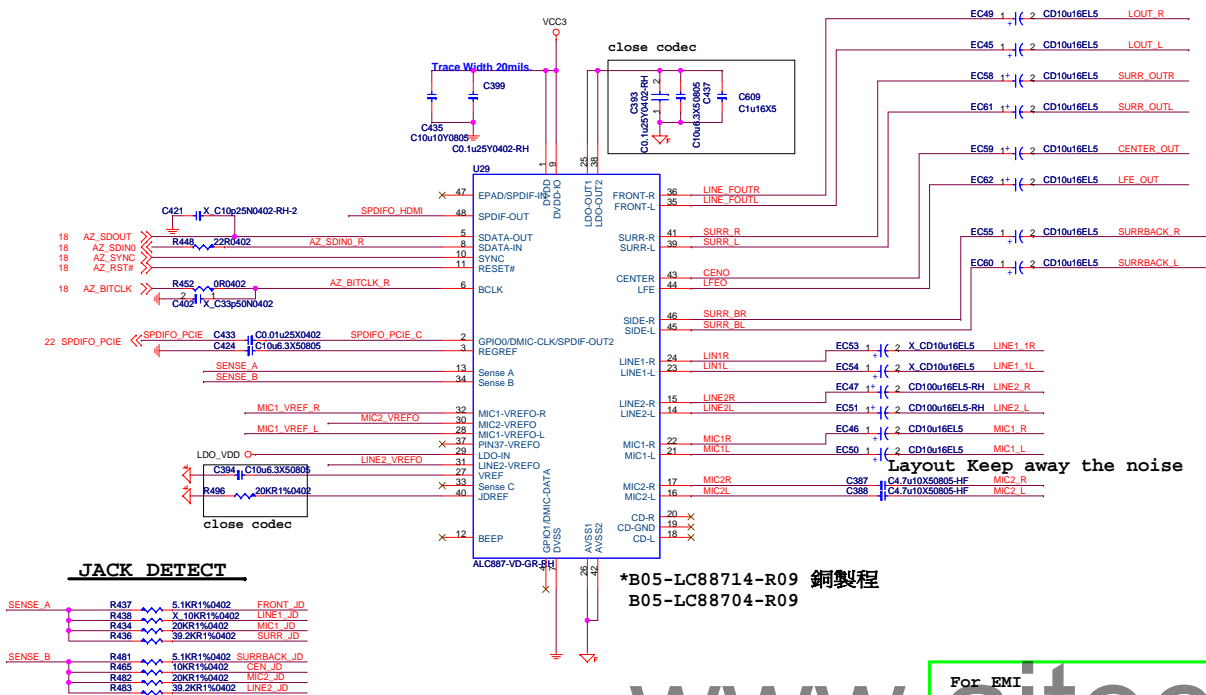
Date: Tuesday, January 11, 2011

Sheet 23 of 42

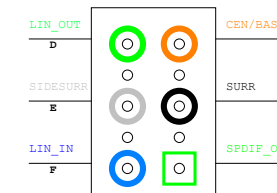
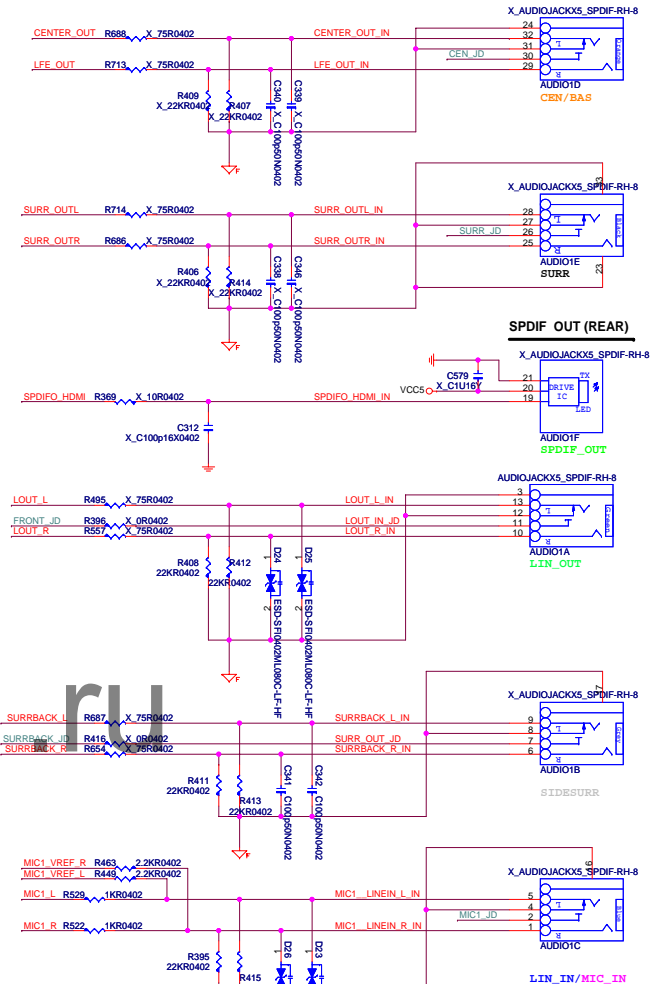
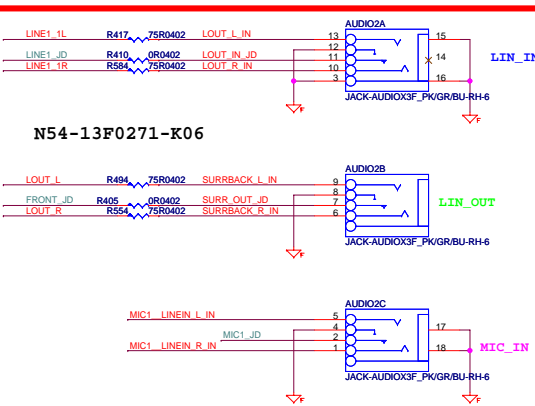
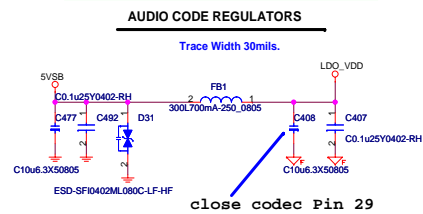
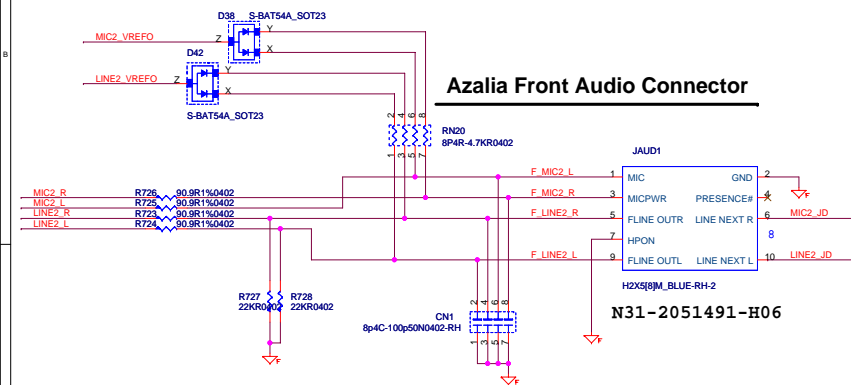
Gigabit LAN INTEL 82579



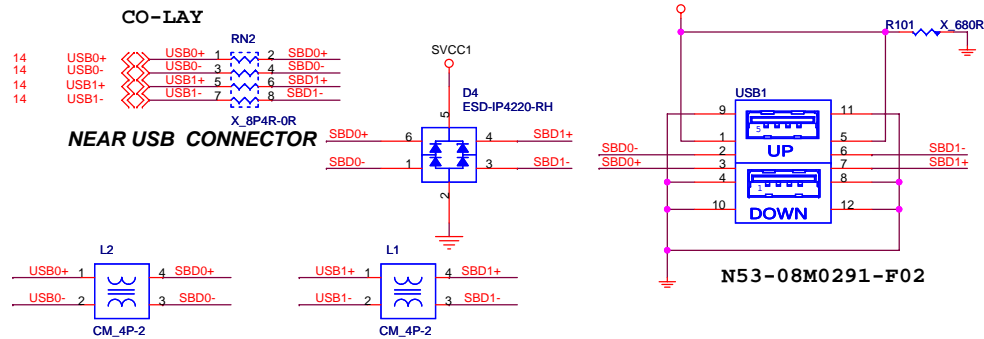
ALC887-VD-GR CODEC



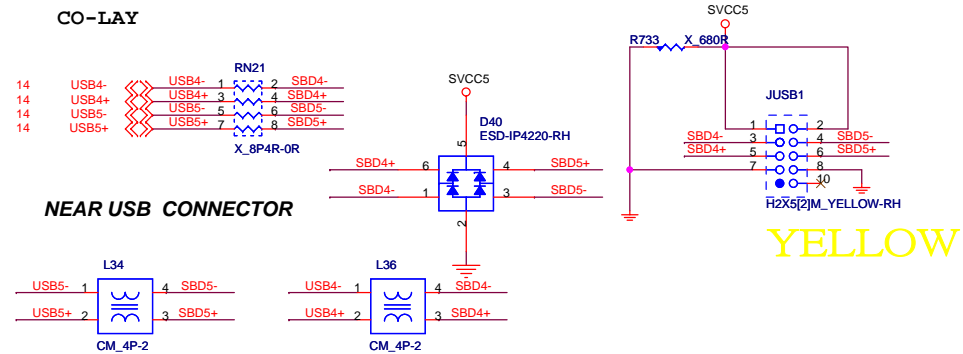
SPDIF_OUT
N32-1030461-H06



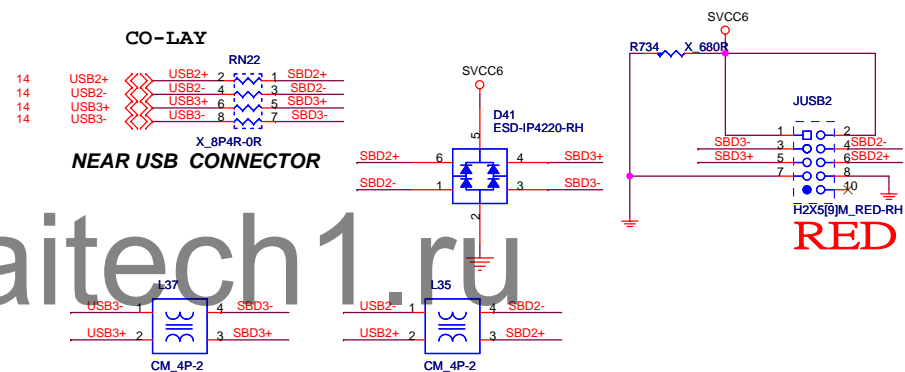
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



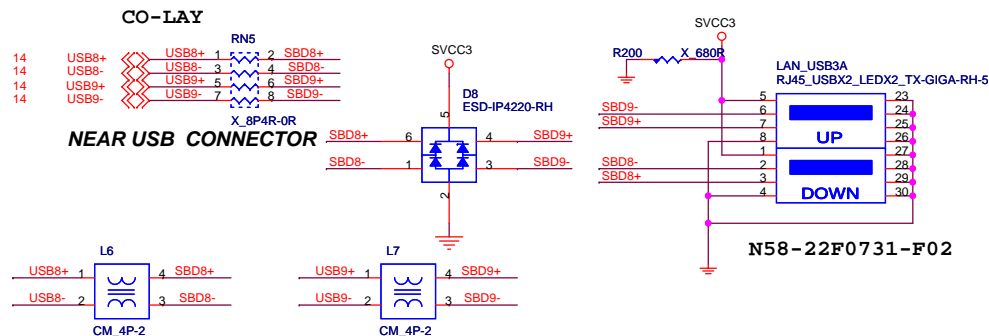
FRONT PANEL USB CONNECTOR FOR USB PORT 12,13



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



REAR PANEL USB CONNECTOR FOR USB PORT 4,5

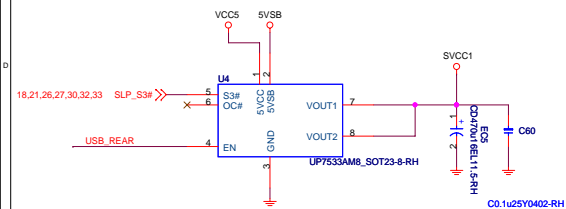


MICRO-STAR INT'L CO.,LTD

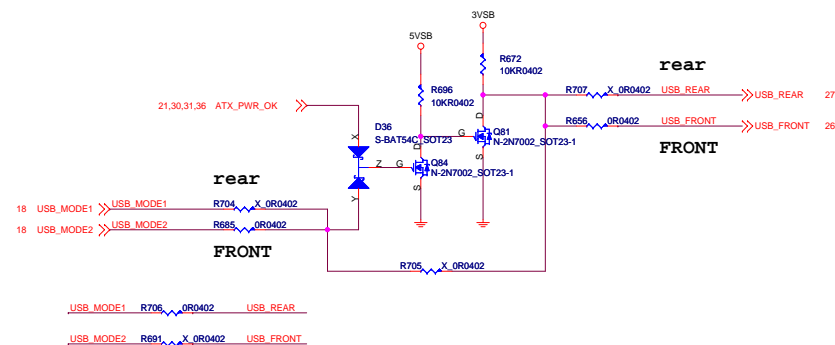
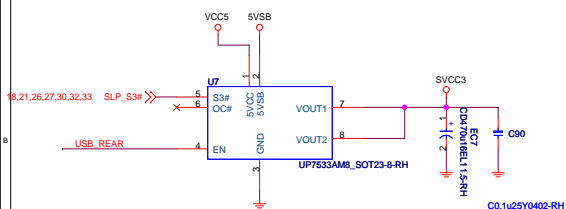
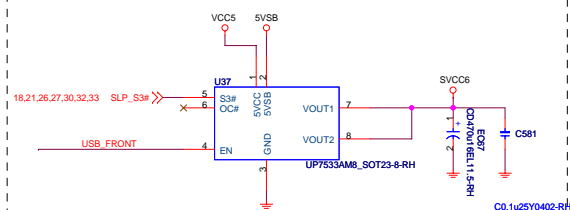
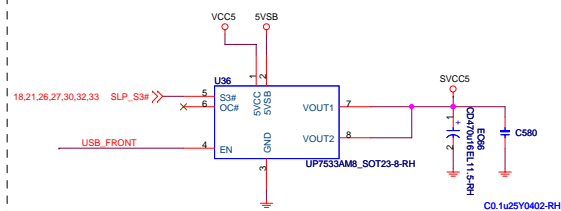
MS-7728

Size	Document Description	Rev
Custom	USB Conn.	10
Date: Tuesday, January 11, 2011	Sheet 28 of 42	

Power Circuit For USB Port 1, 9 (Connector ?) And KB/MS

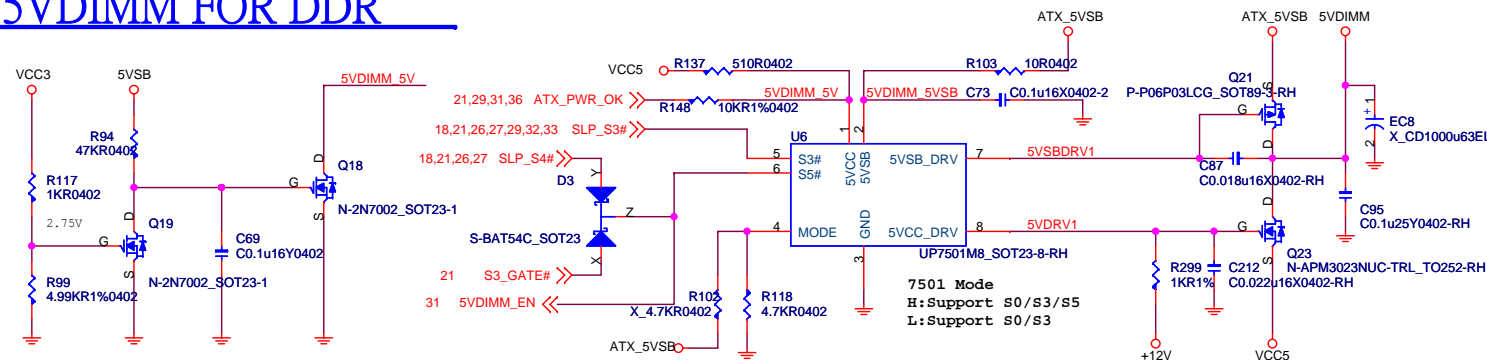


Power Circuit For USB Port 13, 12 (Pin Header ?)

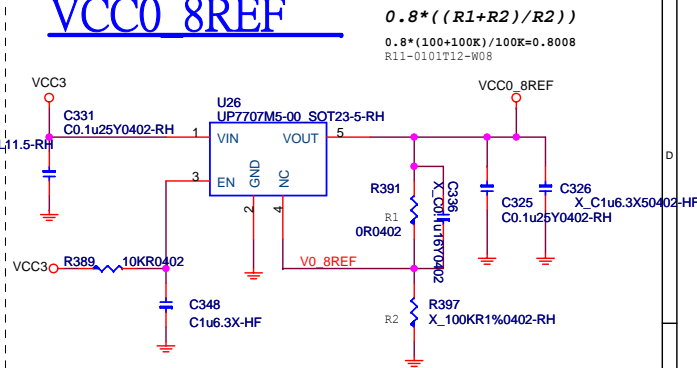


www.aitech1.ru

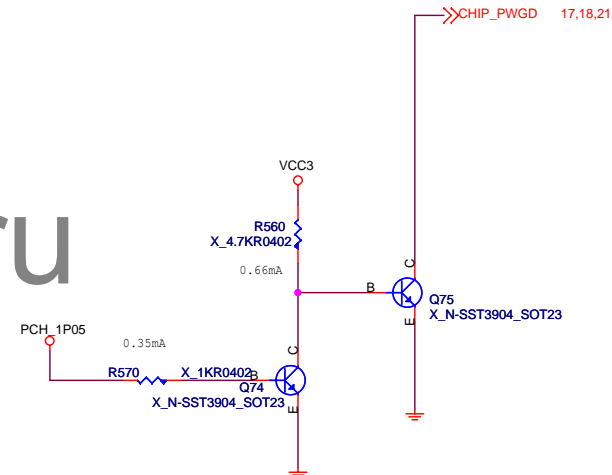
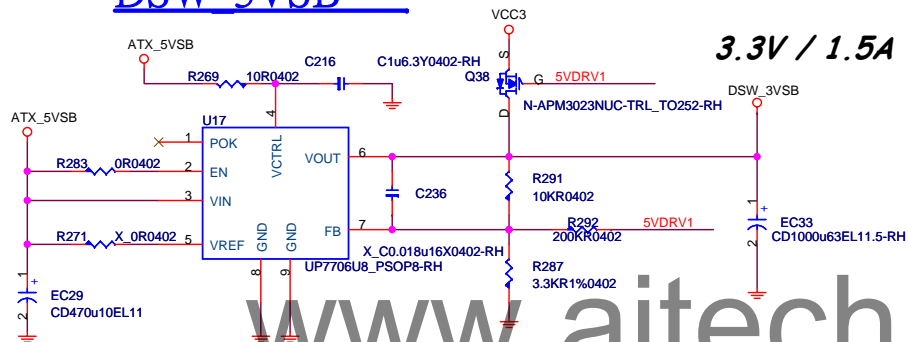
5VDIMM FOR DDR



VCC0 8REF



DSW 3VSB



Update from SLP_S3# to VRM_PGDI



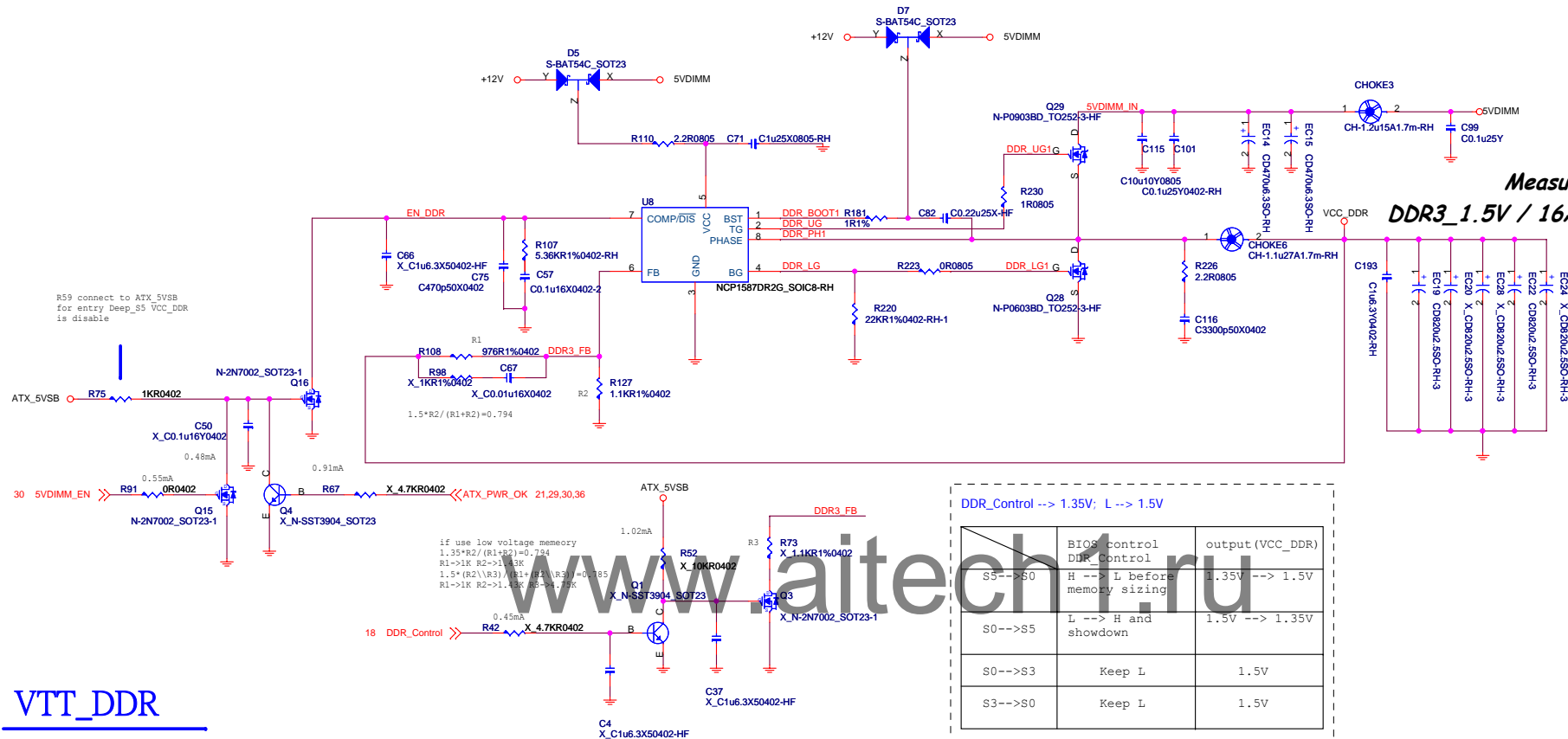
MICRO-STAR INT'L CO.,LTD

MS-7728

Size	Document Description	Rev
B	ACPI Controller 1	10
Date:	Tuesday, January 11, 2011	Sheet 30 of 42

High Side D03-0903B4B-N03
Low Side D03-0603B2B-N03

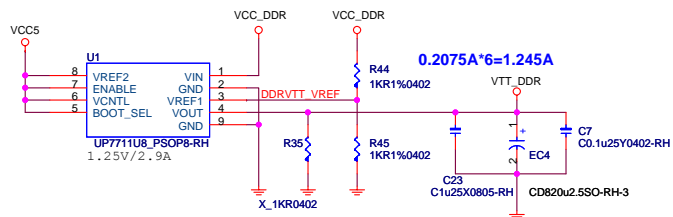
```
D=5/1.5 D=0.3
I=17*0.8 I=13.6A
I ripple=( Io*\sqrt{1-D}) / Phase
I ripple=13.6*0.5477*0.8366
I ripple=6.232A
```



DDR_Control --> 1.35V; L --> 1.5V

S5-->S0	BIOS Control DDR Control H --> L before memory sizing	output (VCC_DDR) 1.35V --> 1.5V
S0-->S5	L --> H and showdown	1.5V --> 1.35V
S0-->S3	Keep L	1.5V
S3-->S0	Keep L	1.5V

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



MICRO-STAR INT'L CO.,LTD

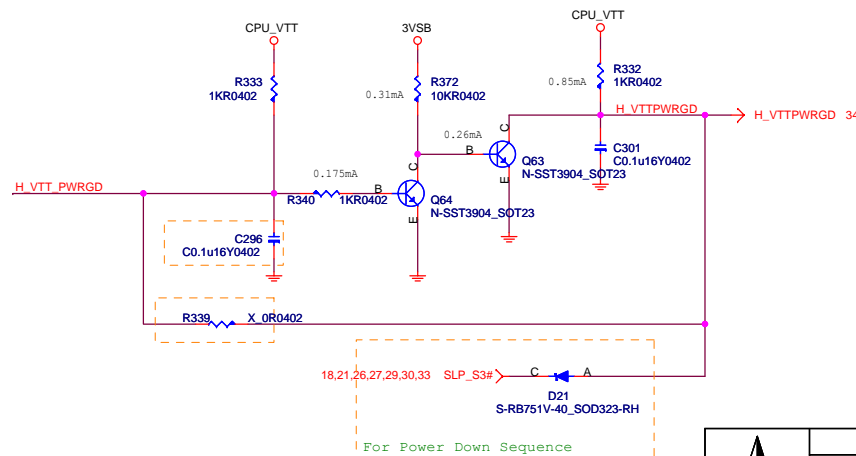
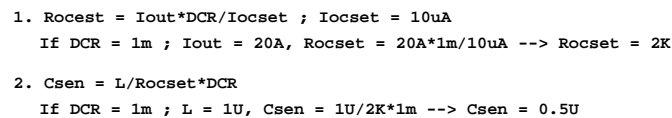
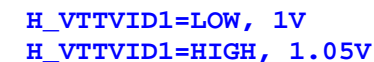
MS-7728

Size Custom	Document Description DDR POWER - NCP1587	Rev 10
Date: Tuesday, January 11, 2011		Sheet 31 of 42

High Side D03-0903B4B-N03
Low Side D03-0603B2B-N03



1.05V/1.00V / 17A



MICRO-STAR INT'L CO.,LTD

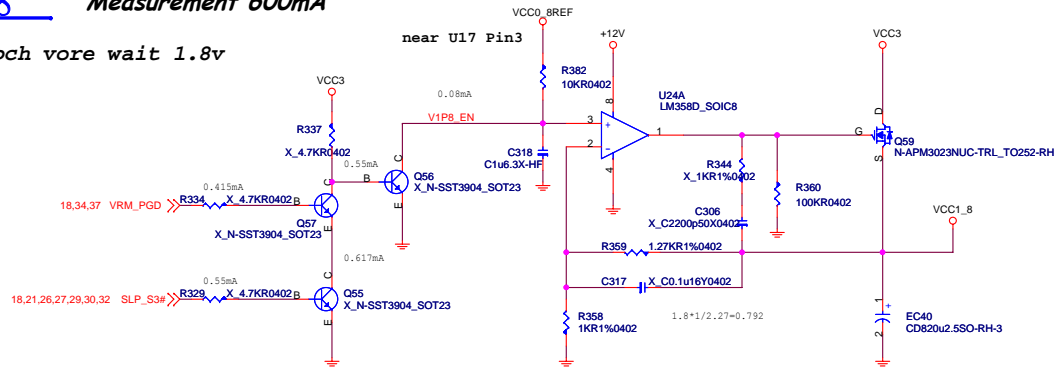
MS-7728

Size	Document Description
Custom	CPU_VTT - NCP5217AMNTXG

Date: Tuesday, January 11, 2011 Sheet 32 of 42

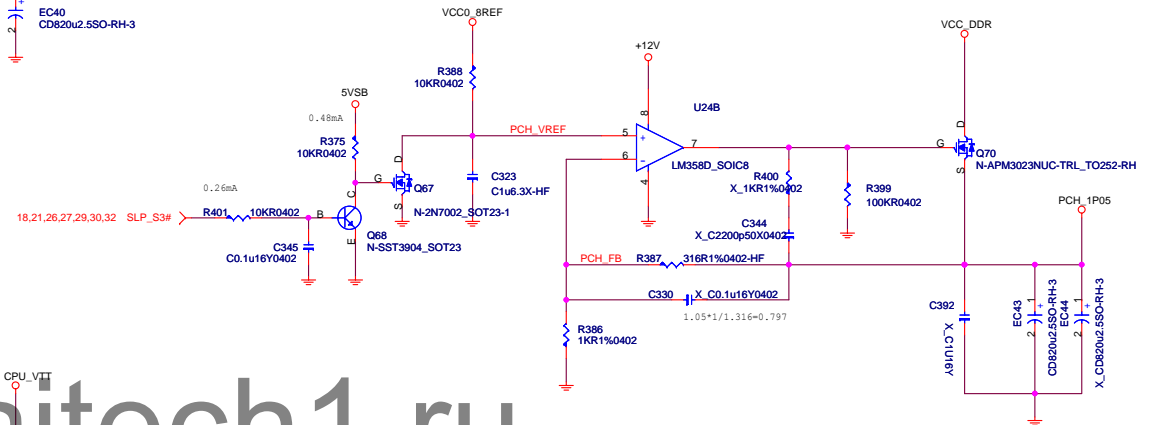
VCC1_8 Measurement 600mA

cpuvt & pch vore wait 1.8v

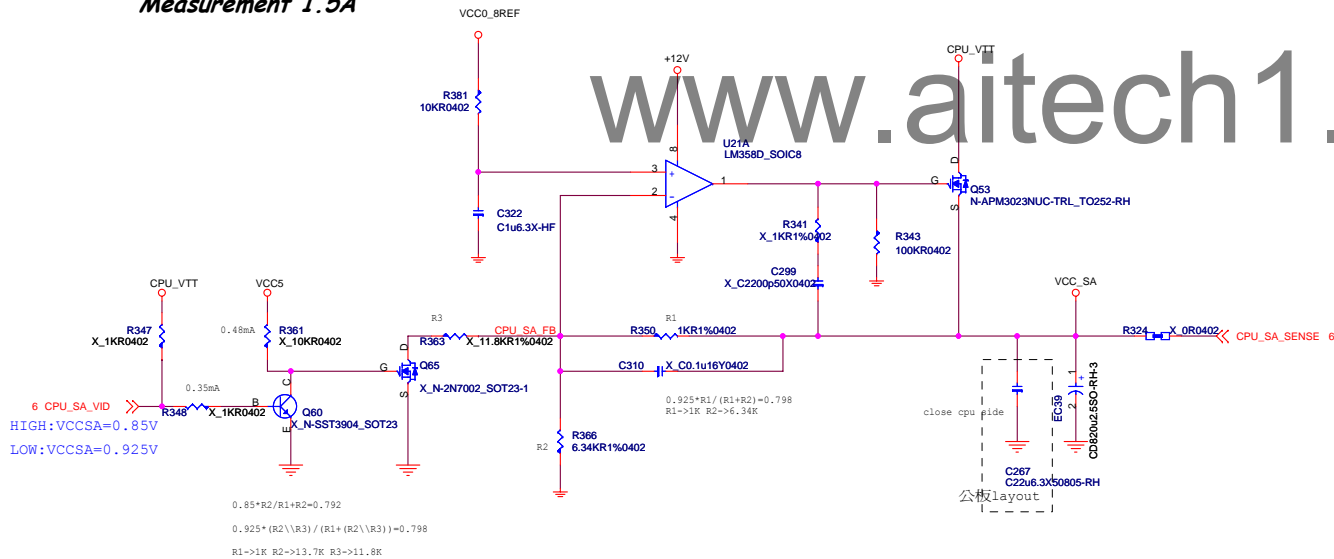


PCH_1P05

1.05V / 6.2A Measurement 4.5A



VCC_SA 0.925V or 0.85V / 8.8A Measurement 1.5A



www.aitech1.ru

Sandy Bridge & Cougar Point Based Platforms
Message of the Week (MOW)
WW32, 2010

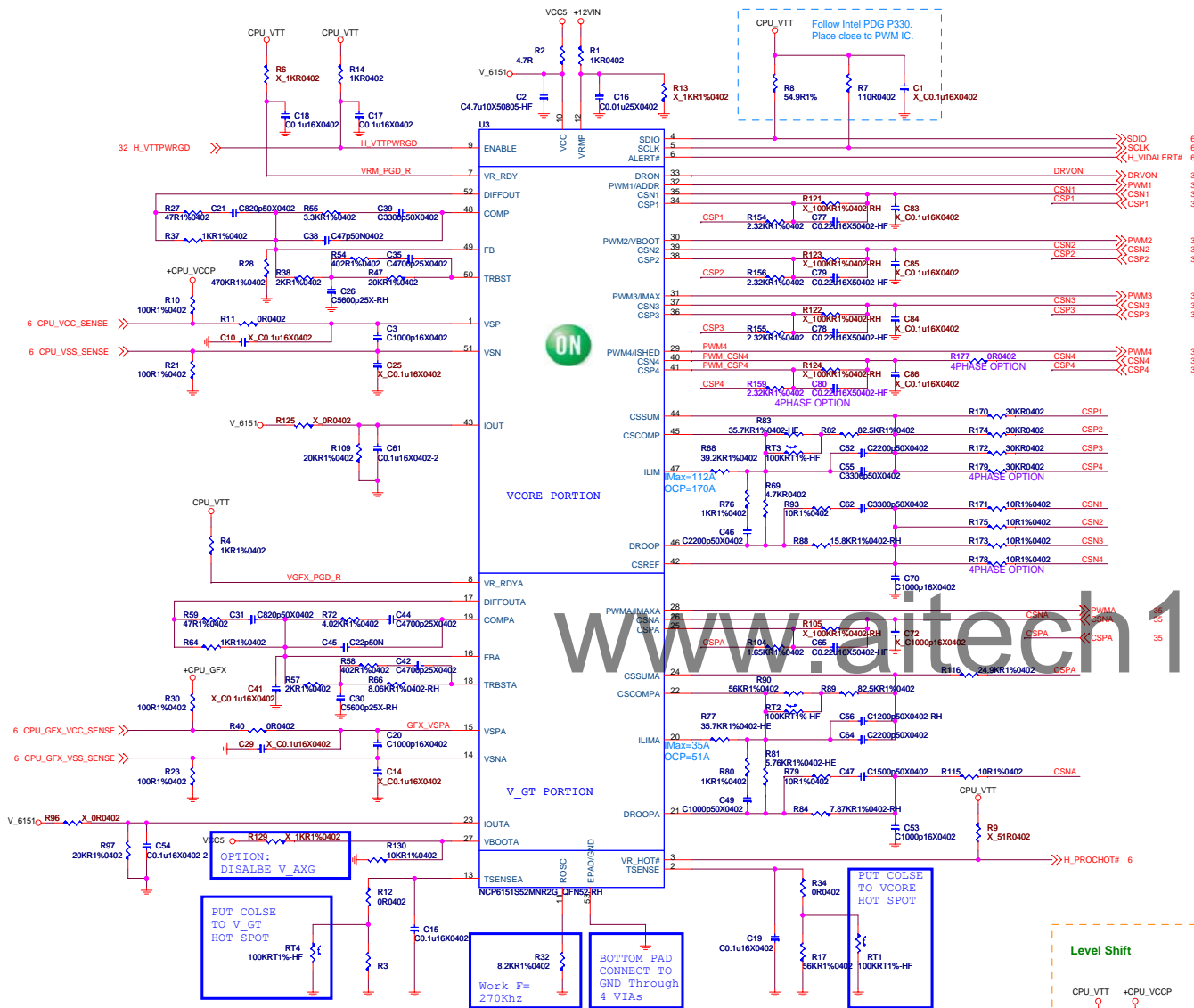
4	VCCIO VR Implementation	Ivy Bridge Compatible: Need to design your VR to be 1.0/1.05V selectable via the VCCIO_SEL pin. No additional VRs needed for compatibility Sandy Bridge only implementation: VCCIO VR can be fixed at 1.05V	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 30.9, Table 30-9
5	VCCSA VR Implementation	Ivy Bridge Compatible: Design your VR to be 0.925/0.85V selectable via VCCSA_VID0 pin. Sandy Bridge only implementation: VCCSA VR can be fixed at 0.925 V.	Refer to Sugar Bay and Bromolow WS Platforms Design Guide – Rev. 1.5, Section 30.9, Table 30-9



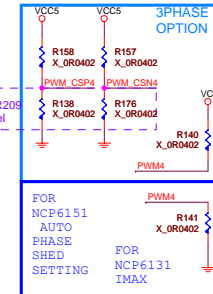
MICRO-STAR INT'L CO.,LTD

MS-7728

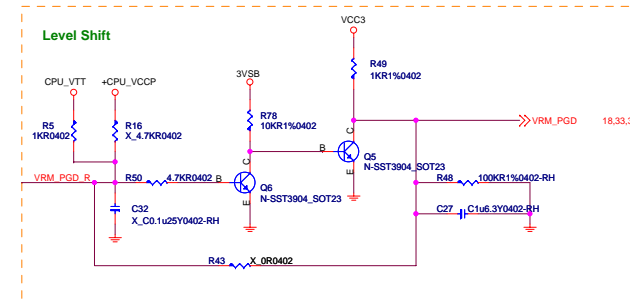
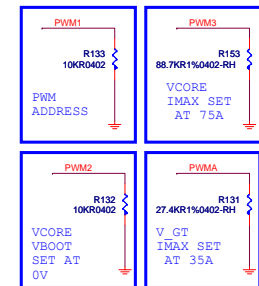
Size Custom	Document Description	Rev 10
	PCH Power-NCP1587D/NCPI02SNT	
Date: Tuesday, January 11, 2011	Sheet 33	of 42



PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101



BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
125K	1.1V
165K	1.5V



High Side D03-0903B4B-N03
Low Side D03-0603B2B-N03

[illegible]

12V FET

C11
C6

C10u25X0805-RH
C10u16X51206-RH

BOOT

R20
2.2R0805

DRVH

SW

DRVL

FLAG/GND

R120
1R0805

R121
10KR

C13
C0.22u25X-HF

DRVHA

10KR

DRVLA

Q10
N-P0603BD_T0252-3-HF

Q11
N-P0603BD_T0252-3-HF

Q14
N-P0903BD_T0252-3-HF

Q13
N-P0903BD_T0252-3-HF

PHASEA

CH01
0.5u35A1.5m-HF

CH02

CH0.5u35A1.5m-HF

R71
2.2R0805

C34
C2200p16X0402

CP10
CP13
X_COPPER
X_COPPER

CSPA

34

BOTTOM PAD CONNECT TO GND Through 4 VIAs

Diagram illustrating the power supply connection for the +CPU_GFX. The circuit shows four parallel branches, each containing a 10k resistor and a 2.5SO-RH-3 component. The components are labeled EC13, EC11, EC6, and EC12. The ground connection is shown at the bottom right.

N93-04M0221-H06

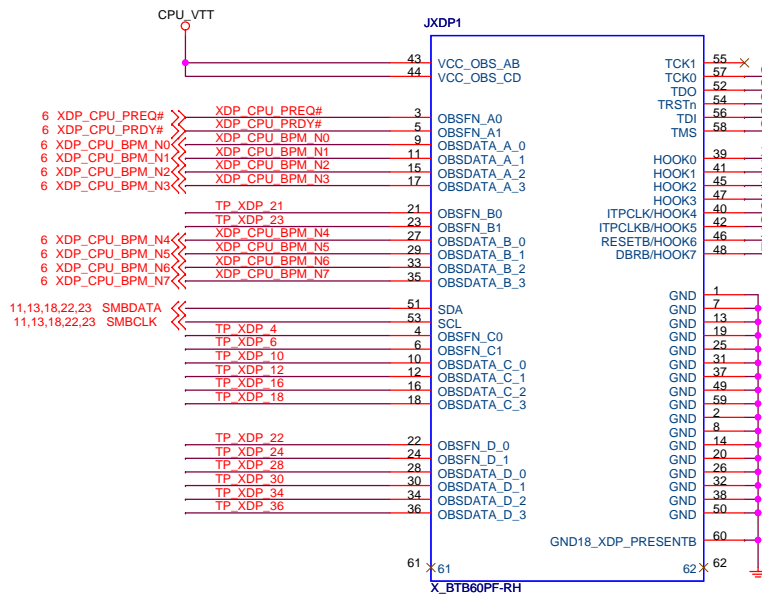
Caps

Diagram illustrating the power plane layout for the +CPU_VCCP supply. The layout shows a grid of decoupling capacitors connected to the +CPU_VCCP rail and a common ground plane.

Capacitors and their values:

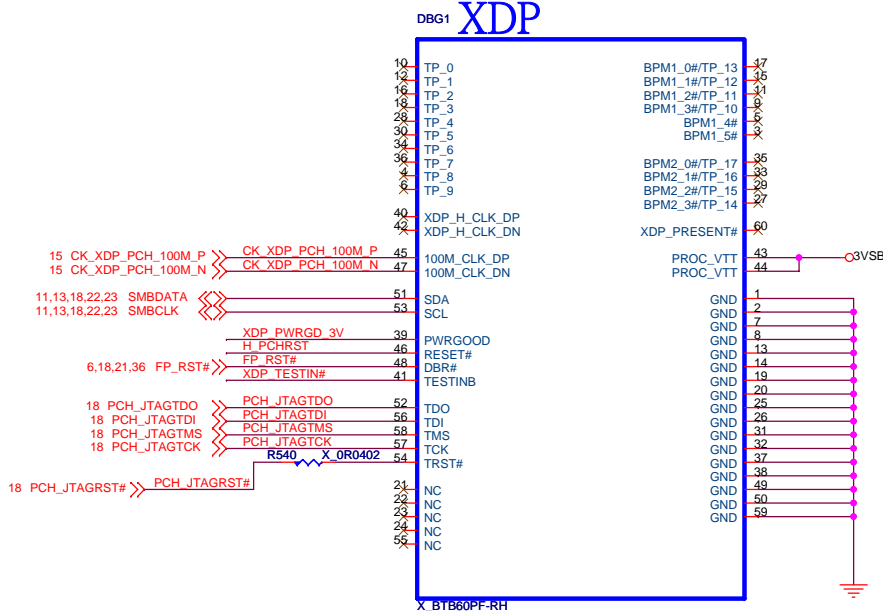
- EC10: 2 x CD820u2 550-RH-3
- EC9: 2 x CD820u2 550-RH-3
- EC31: 2 x CD820u2 550-RH-3
- EC27: 2 x CD820u2 550-RH-3
- EC21: 2 x CD820u2 550-RH-3
- EC18: 2 x CD820u2 550-RH-3
- EC17: 2 x CD820u2 550-RH-3

CPU
XDP



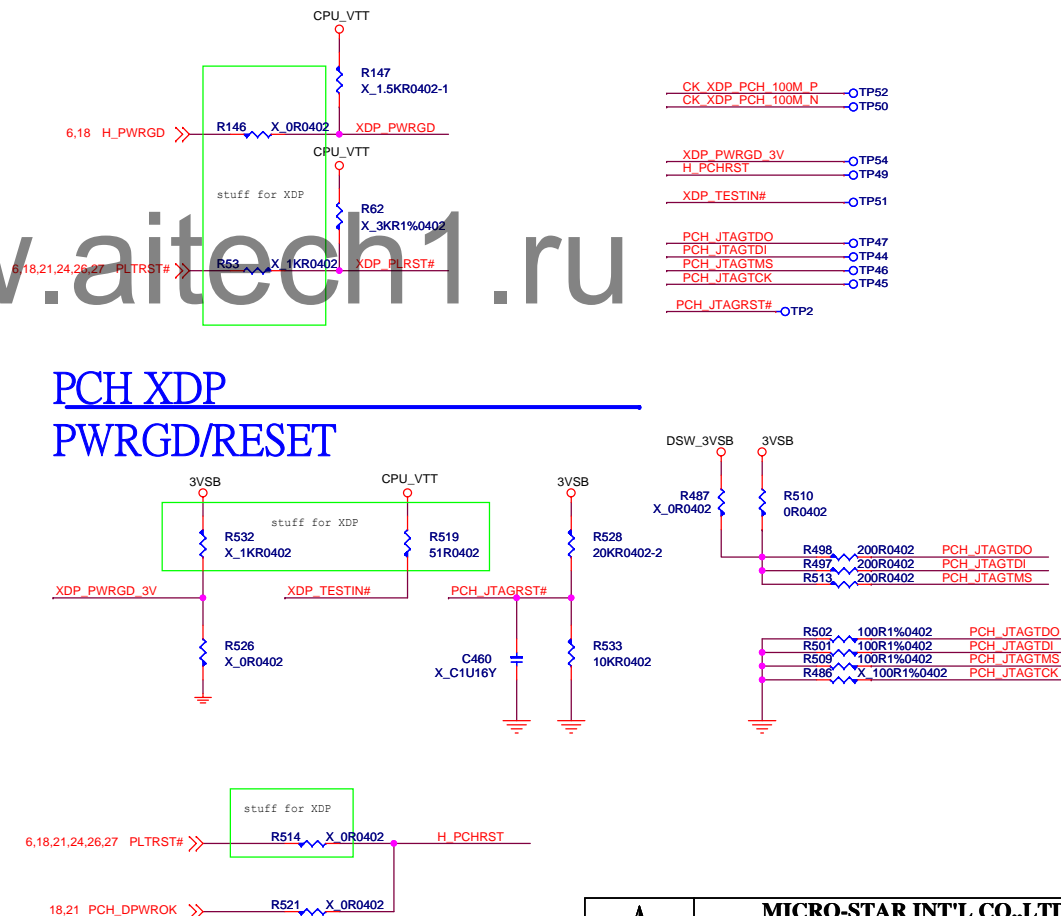
N5C-60F0040-S88

PCH
XDP¹



N5C-60F0040-S88

PCH XDP
PWRGD/RESET

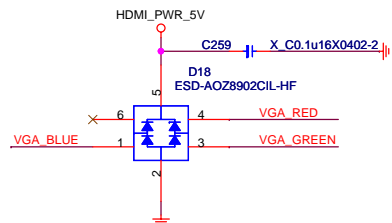
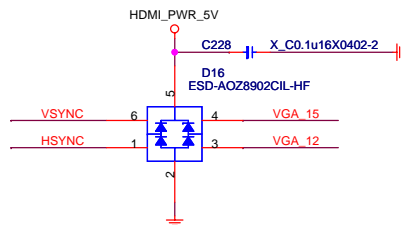
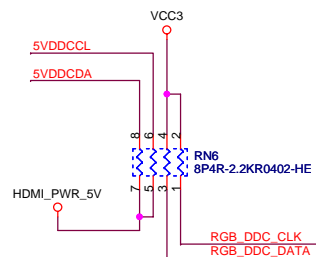
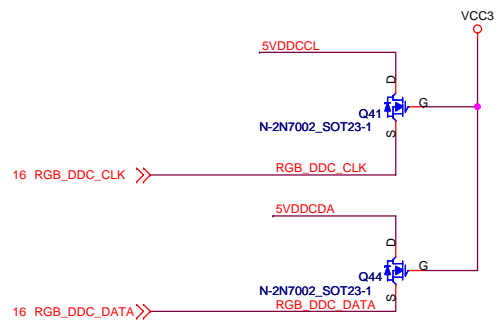


MICRO-STAR INT'L CO.,LTD

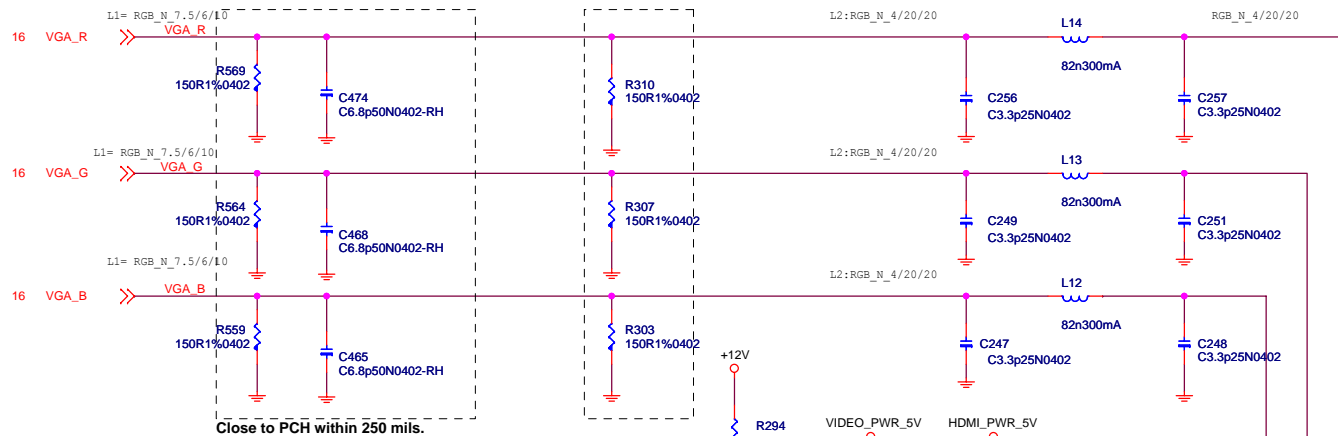
MS-7728

Size Custom	Document Description CPU/PCH XDP	Rev 10
Date: Tuesday, January 11, 2011		Sheet 37 of 42

Video Connector



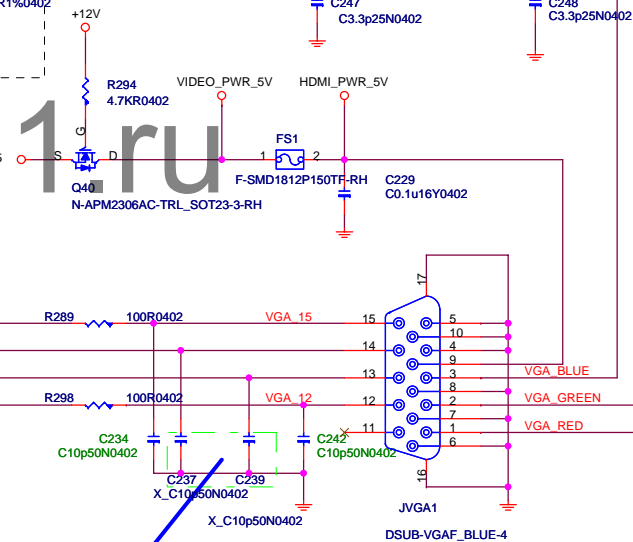
PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



www.aitech1.ru

CLOSE TO PCH

Close to PCH within 750 mils.



not stuff C237 C239 for SA D_SUB check fail

N51-15F0371-I60

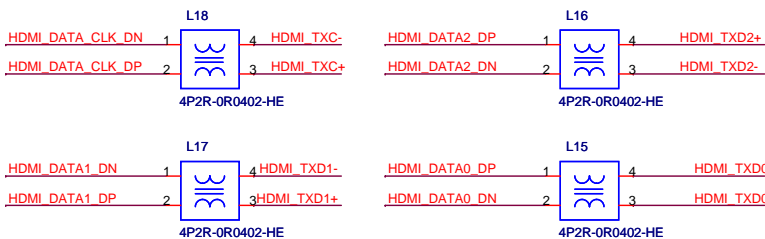
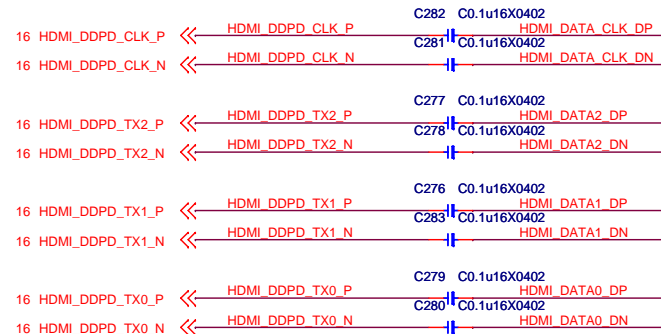


MICRO-STAR INT'L CO.,LTD

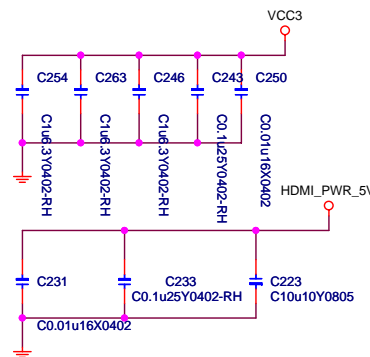
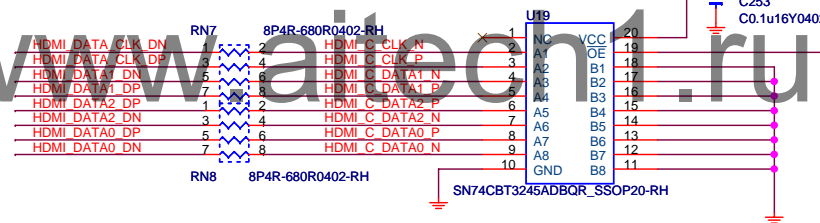
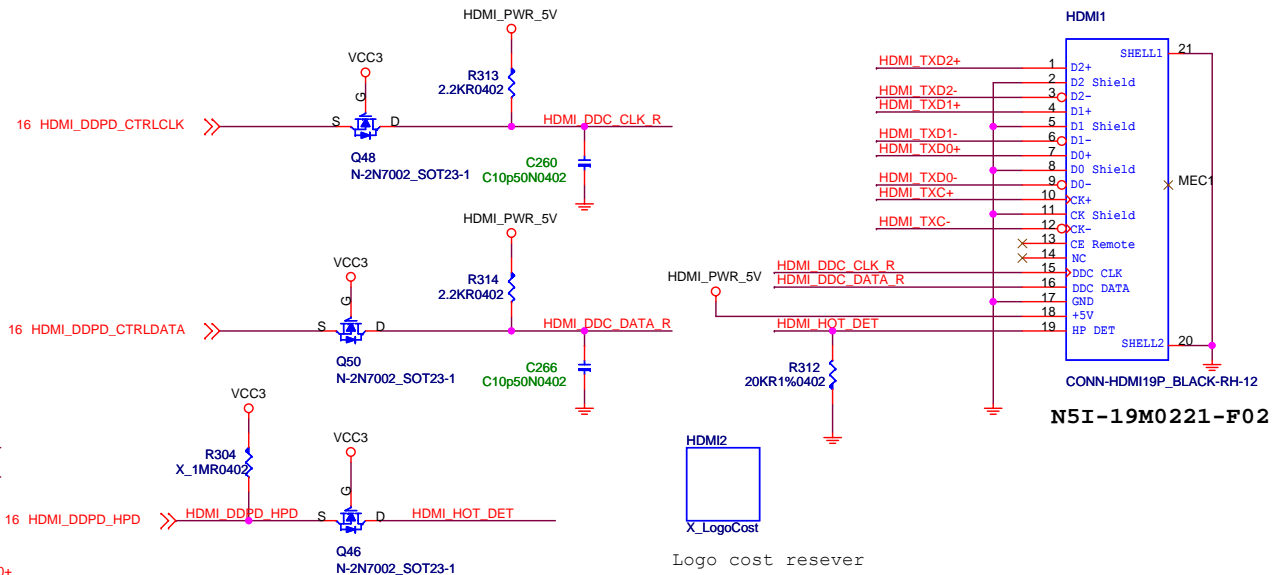
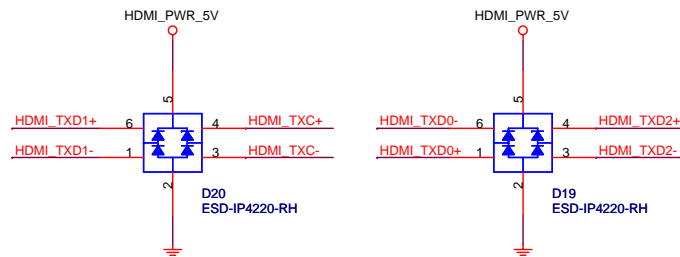
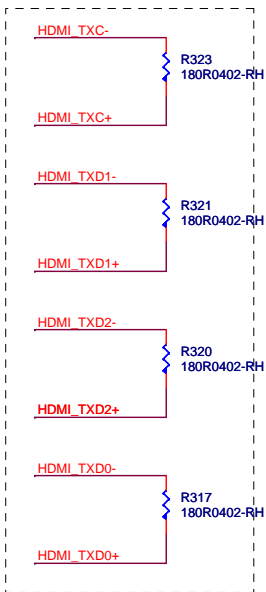
MS-7728

Size	Document Description	Rev
Custom	DESCRIPTION	10
Date:	Tuesday, January 11, 2011	Sheet 38 of 42

HDMI level shifter



EMI Close to connector



MICRO-STAR INT'L CO.,LTD

MS-7728

Size B	Document Description	Rev 10
	HDMI transfer	
Date: Tuesday, January 11, 2011	Sheet 39 of 42	

ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

CPU PW
12V +/-5%

VRD12 +CPU_VCCP PWM REGULATOR
--

+CPU_GFX PWM REGULATOR

+CPU_VTT PWM REGULATOR

+CPU_VCCSA PWM REGULATOR

5V_DIMM Linear REGULATOR

VCC_DDR PWM REGULATOR

PCH_1P05 PWM REGULATOR

5V_USB Linear REGULATOR

3VSB Linear REGULATOR

X1 PCIe per
+3.3V 3.0A
+12V 0.5A
+3.3Vaux 0.4A

X16 PCIe
+3.3V 3.0A
+12V 5.5A
+3.3Vaux 0.4A

USB3.0 X2 FR
VDD
5V_USB
2.0A

USB3.0 X2 RL
VDD
5V_USB
2.0A

USB X6 FR
VDD
5V_USB
3.0A

USB X6 RL
VDD
5V_USB
3.0A

SANDY BRIDGE (95W)
VCCP (CPU core series VID) 112A
VAXG (GFX core) 35A
VTT (CPU Uncore, I/O) 8.5A
VCCSA (CPU Uncore, I/O) 8.8A
VDDQ (DDR I/O) 4.5A
VccPLL (SFR supplies) 1A

Cougar Point PCH (5.5W)
V_CPU_CORE 1.05V 6.2A
VccPLL 1.05V 0.5A
Vcc3_3 3.3V 0.203A
V5REF 5V <1mA
V5REF_Sus 5V <1mA
Vcc3_3SB 3.3V 0.123A
VccADAC 3.3V 60mA
VccRTC 3.3V <1mA

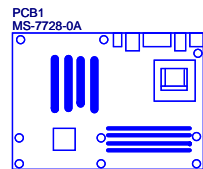
HD Audio 92HD89E
+5VR 51 mA
VCC3 40 mA

LAN RTL8111E
VDD3 58mA
VDD1P2 289mA



MICRO-STAR INT'L CO.,LTD		
MS-7728		
Size Custom	Document Description Power Delivery	Rev 10
Date: Tuesday, January 11, 2011	Sheet 40 of 42	

PCB



Main : P30-0772810-G37
Avl : P30-0772810-E36

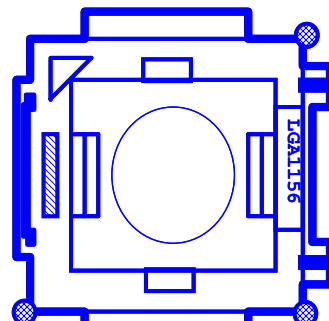


BAT-BCR2032P-RH



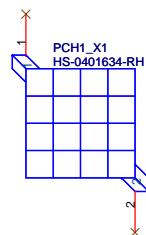
CPU SOCKET

CPU1_X1
CPU SOCKET



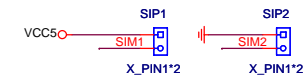
E21-7557010-F02

NB Heat-sink

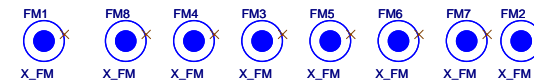


E31-0401634-K08

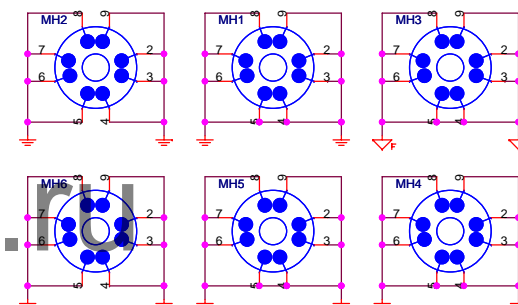
Simulation



Optical Fiducial Marks-120



Mounting Holes



MICRO-STAR INT'L CO.,LTD

MS-7728

Size Custom Document Description
Manual & Option parts

Rev 10

Date: Tuesday, January 11, 2011

Sheet 41 of 42

2010-11-16

R_VCC_1P05:R280-->3.16K 1% R279-->1K1%
F_VCC_1P05:R606-->3.16K 1% R615-->1K1%
CPU_GFX no power-->remove R129
BOM 轉正式料號OL4-7479002 --> L04-03A7151-L65
CHOKE1,5,7,8

2010-12-23

- 1.HDMI 線路 將RN7 RN8 擺放置 U19 前面
- 2.KB/MS add D43 ESD
- 3.LAN Power 線路 add Q88 Q87 C608 C607 C606 C605 R737 fix Lan power rise time fast issue

2010-12-28

power solution remove C589 C588
MS-7728-1.0 CFG-7728-1.0-USBF + 3 hole audio
R681 stuff Q80 R671 don't stuff fix power sequence fail issue

2010-12-29


SIO add R738 0ohm, not stuff D29
audio Pin38 add C609 1uF 0603 X5R

2010-01-06

C237,C239 not stuff fix VGA issue
上蓋: E21-7557050-L06
底座: N12-155A010-L06

CFG	BOM	
CFG-7728-10-USBF	601-7728-01S	Front USB3.0 + 3 hole AUDIO
CFG-7728-10-USBR	601-7728-02S	Rear USB3.0 + 3 hole AUDIO

www.aitech1.ru



MICRO-STAR INT'L CO.,LTD

MS-7728

Size Custom	Document Description History	Rev 10
Date: Tuesday, January 11, 2011		Sheet 42 of 42